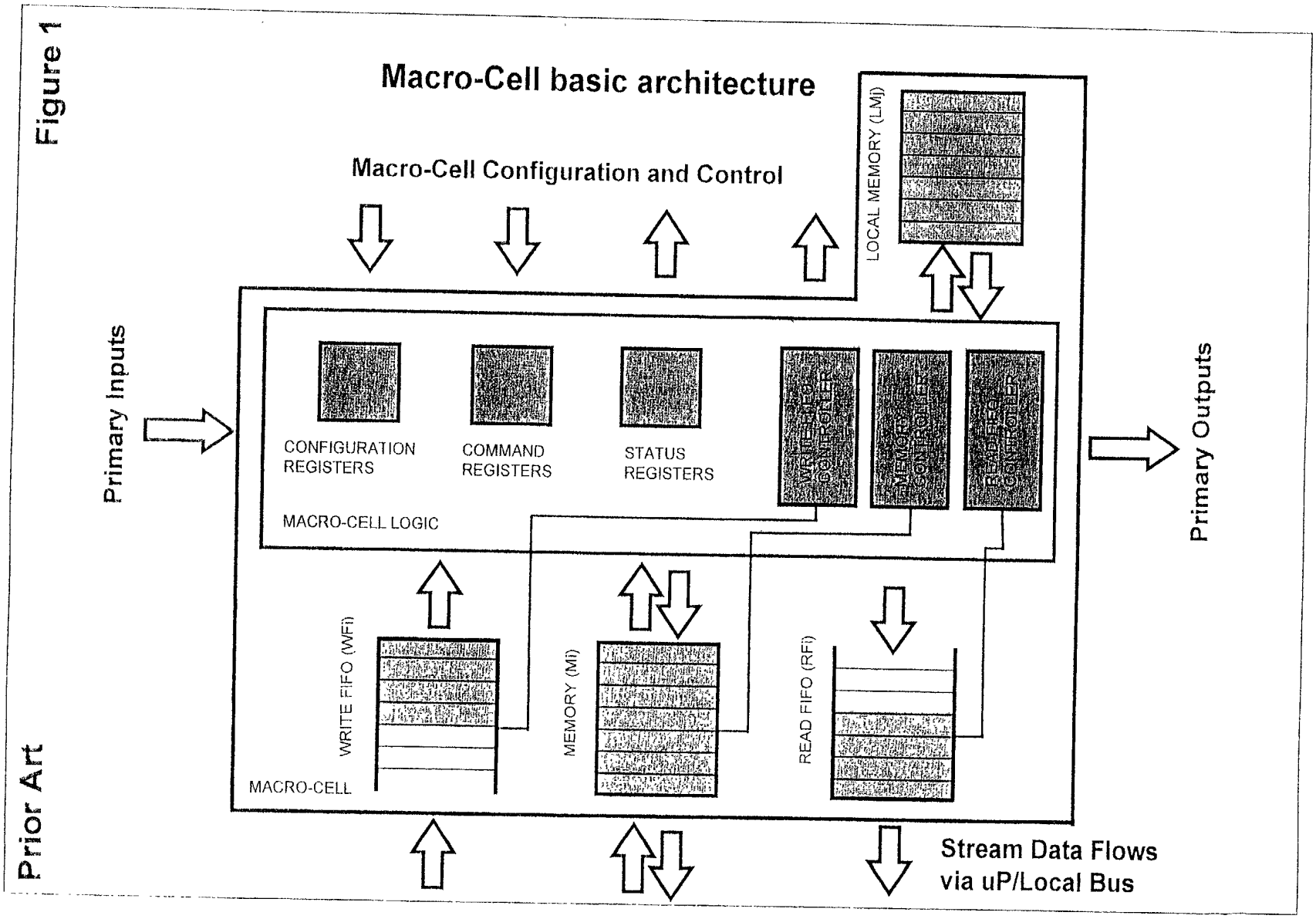
Figure 1



Prior Art

Figure 2

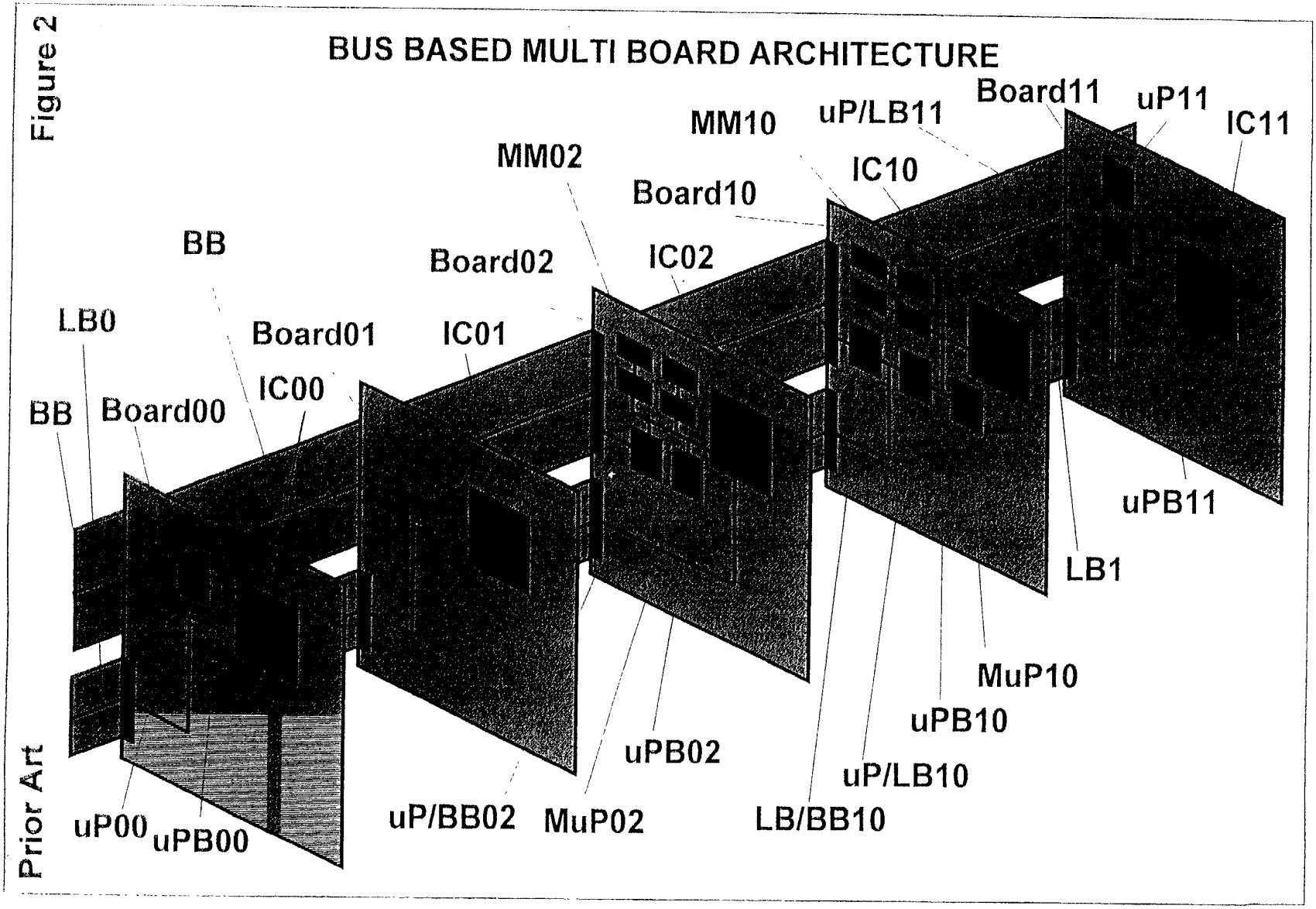
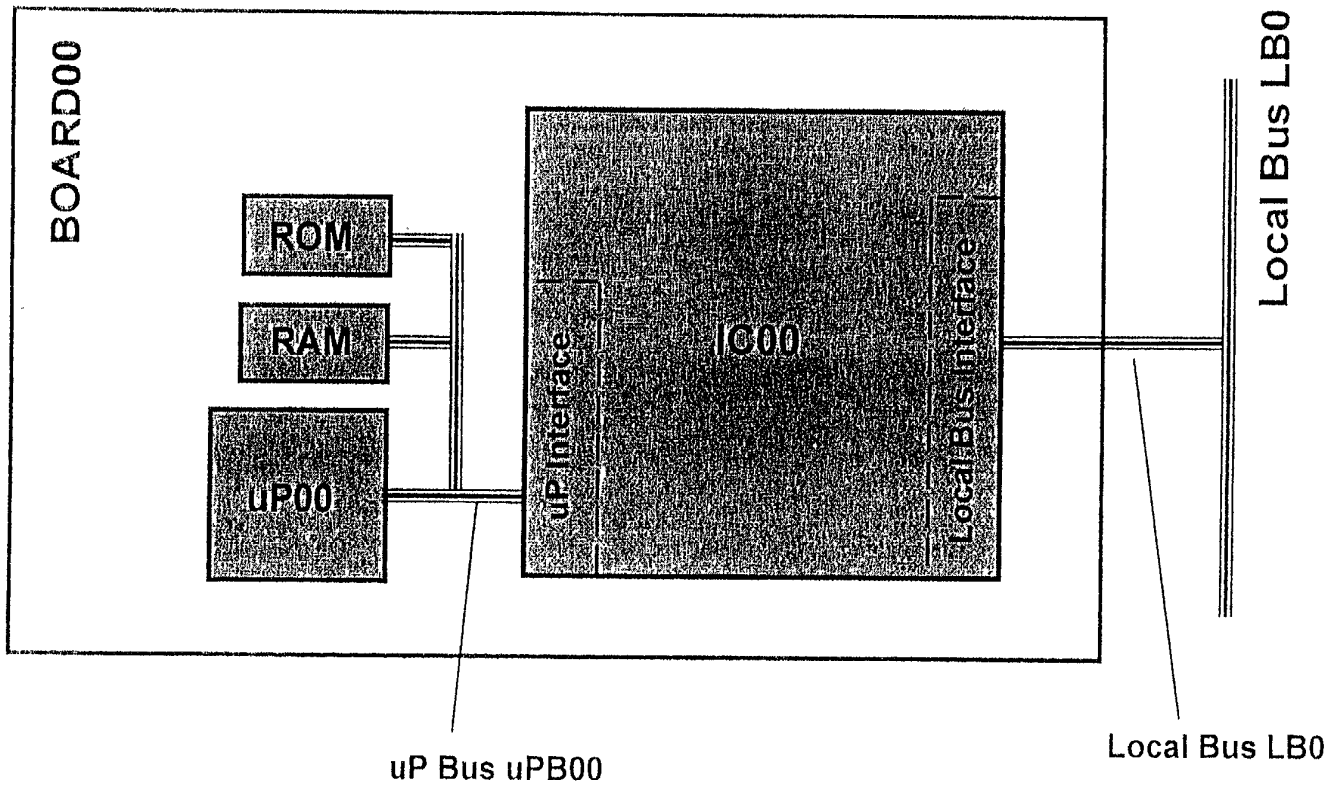


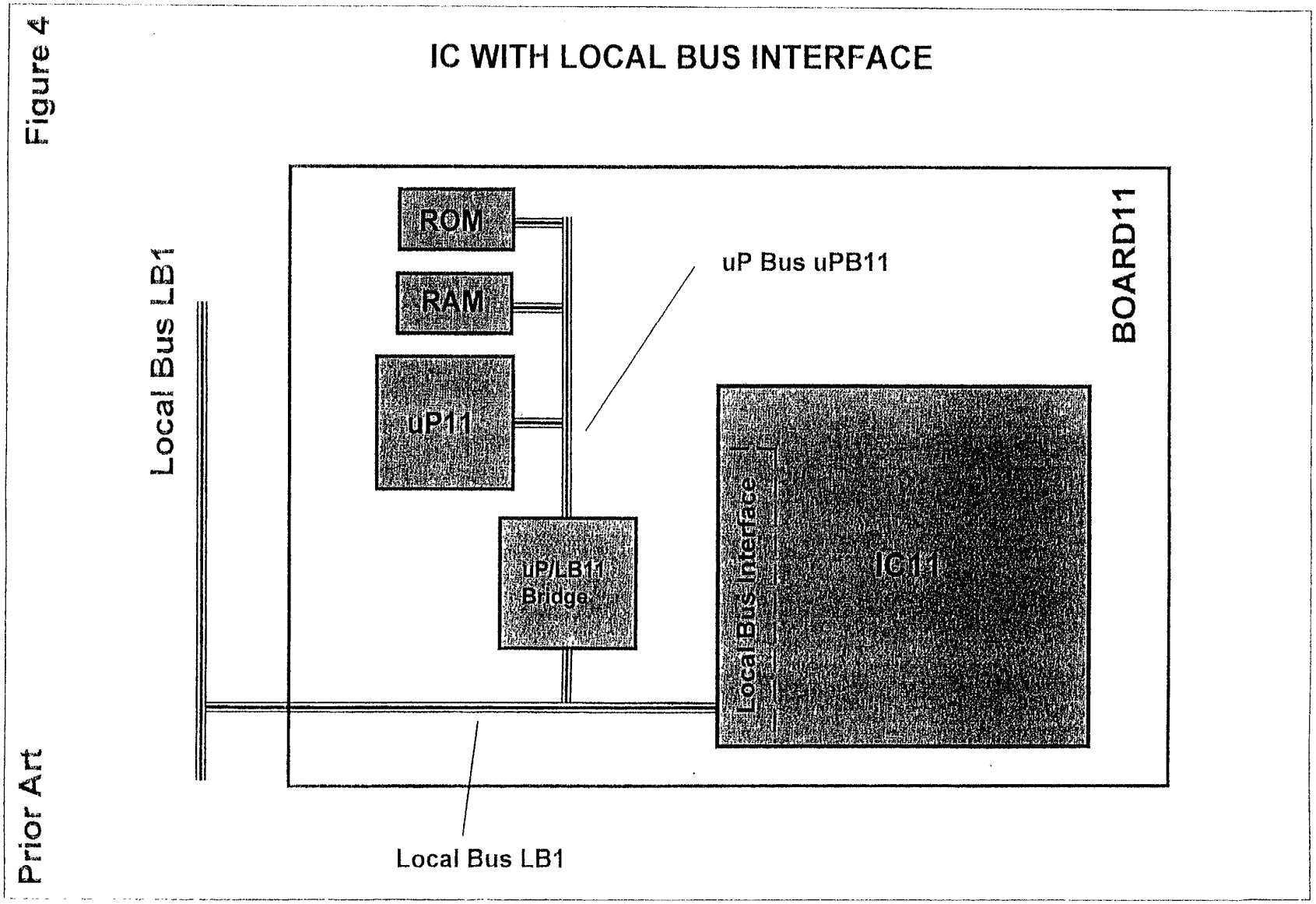
Figure 3

IC WITH uP INTERFACE AND LOCAL BUS INTERFACE



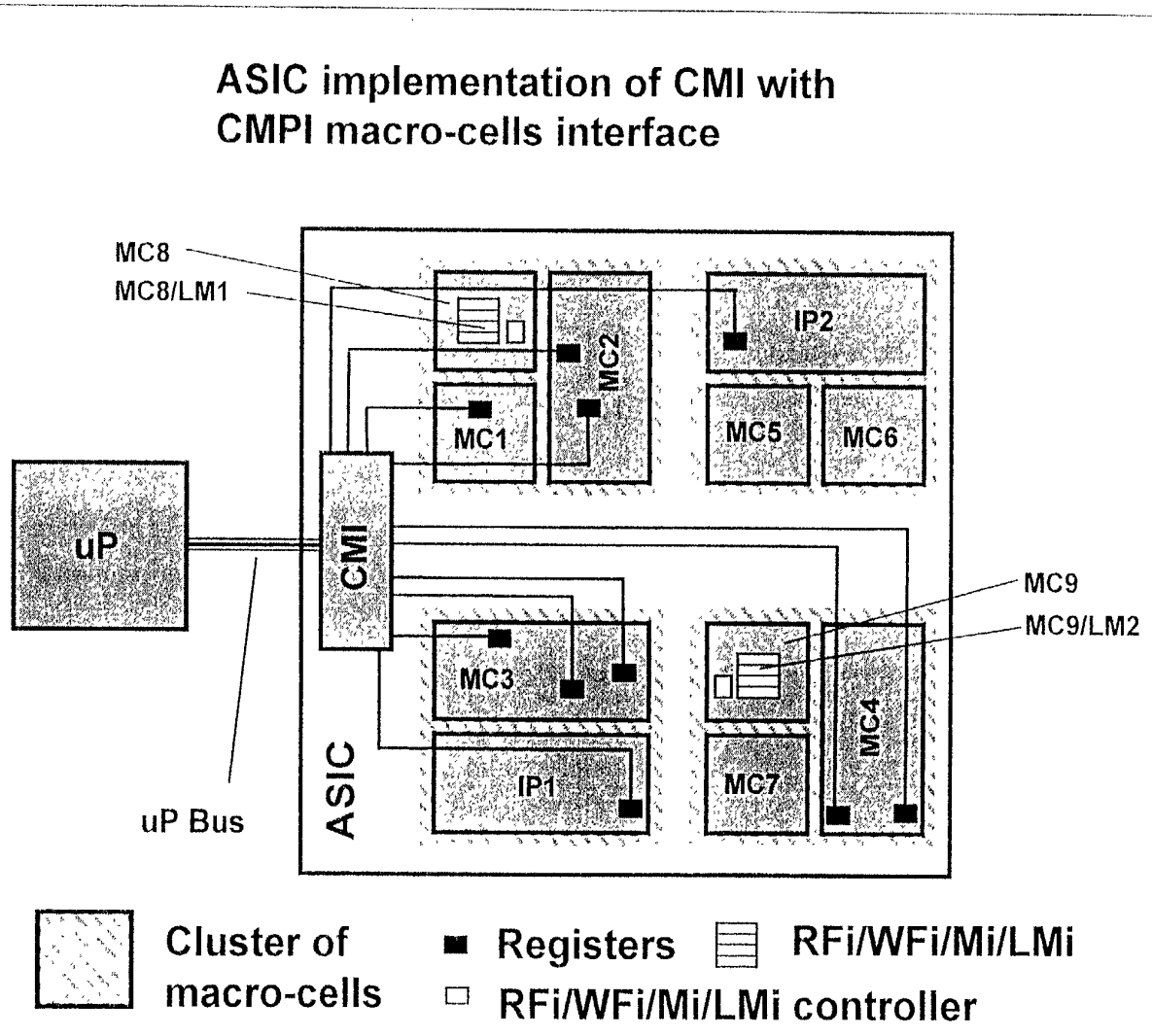
Prior Art

Figure 4



Prior Art

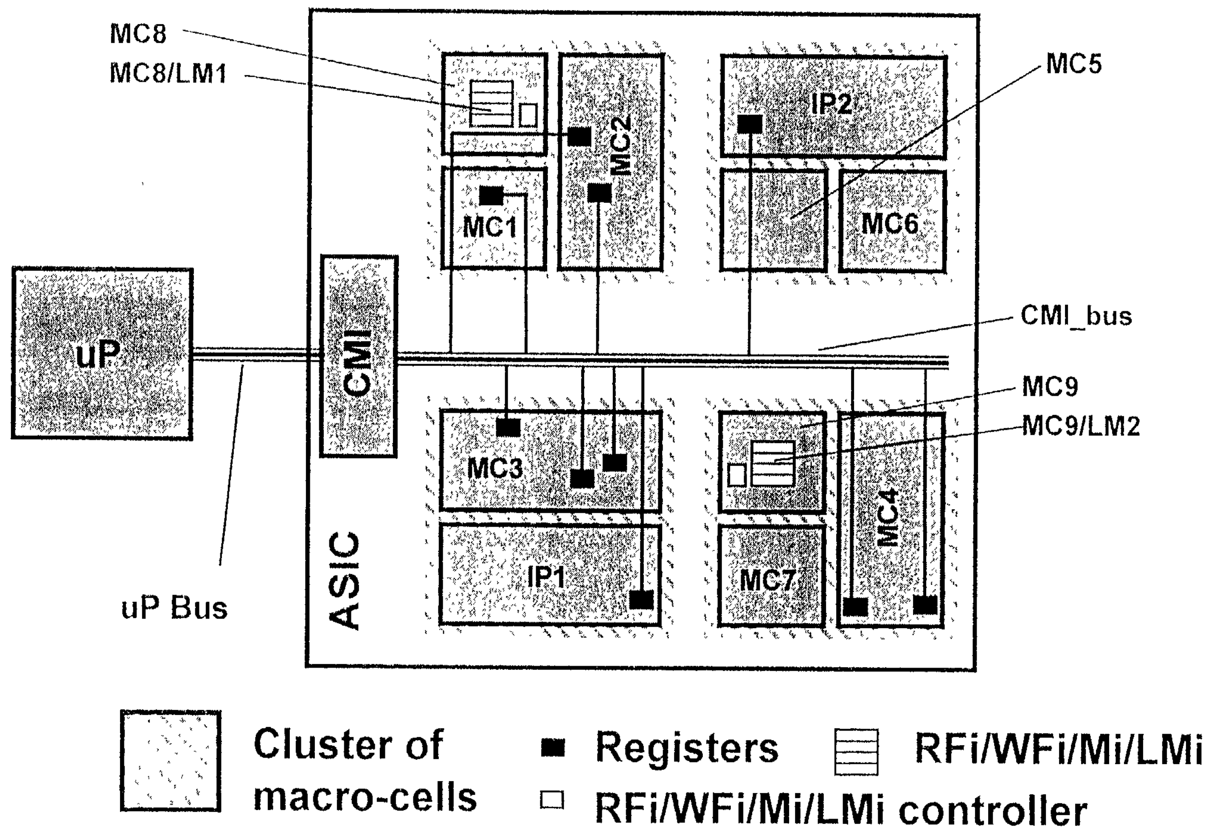
Figure 5



Prior Art

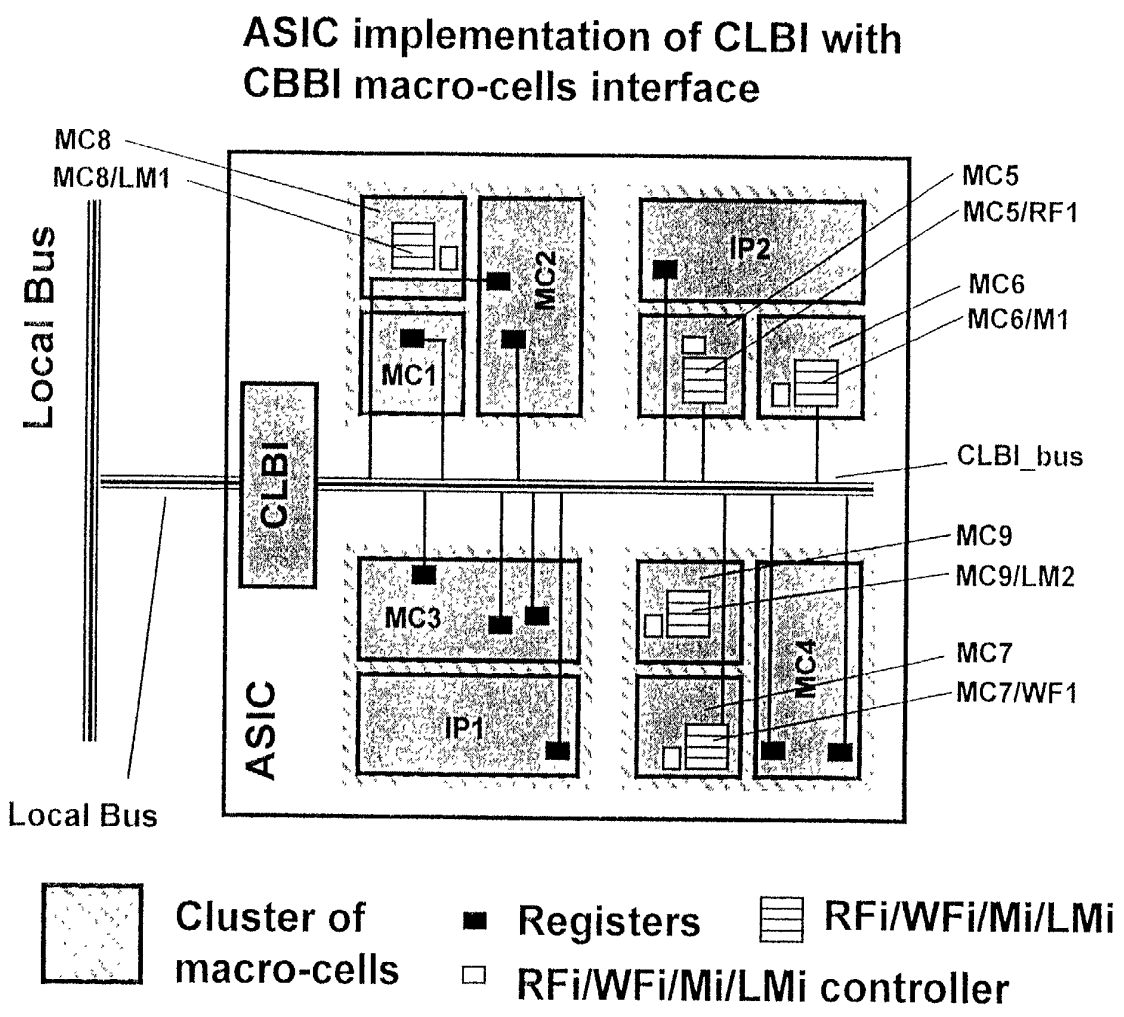
Figure 6

ASIC implementation of CMI with CBBI macro-cells interface



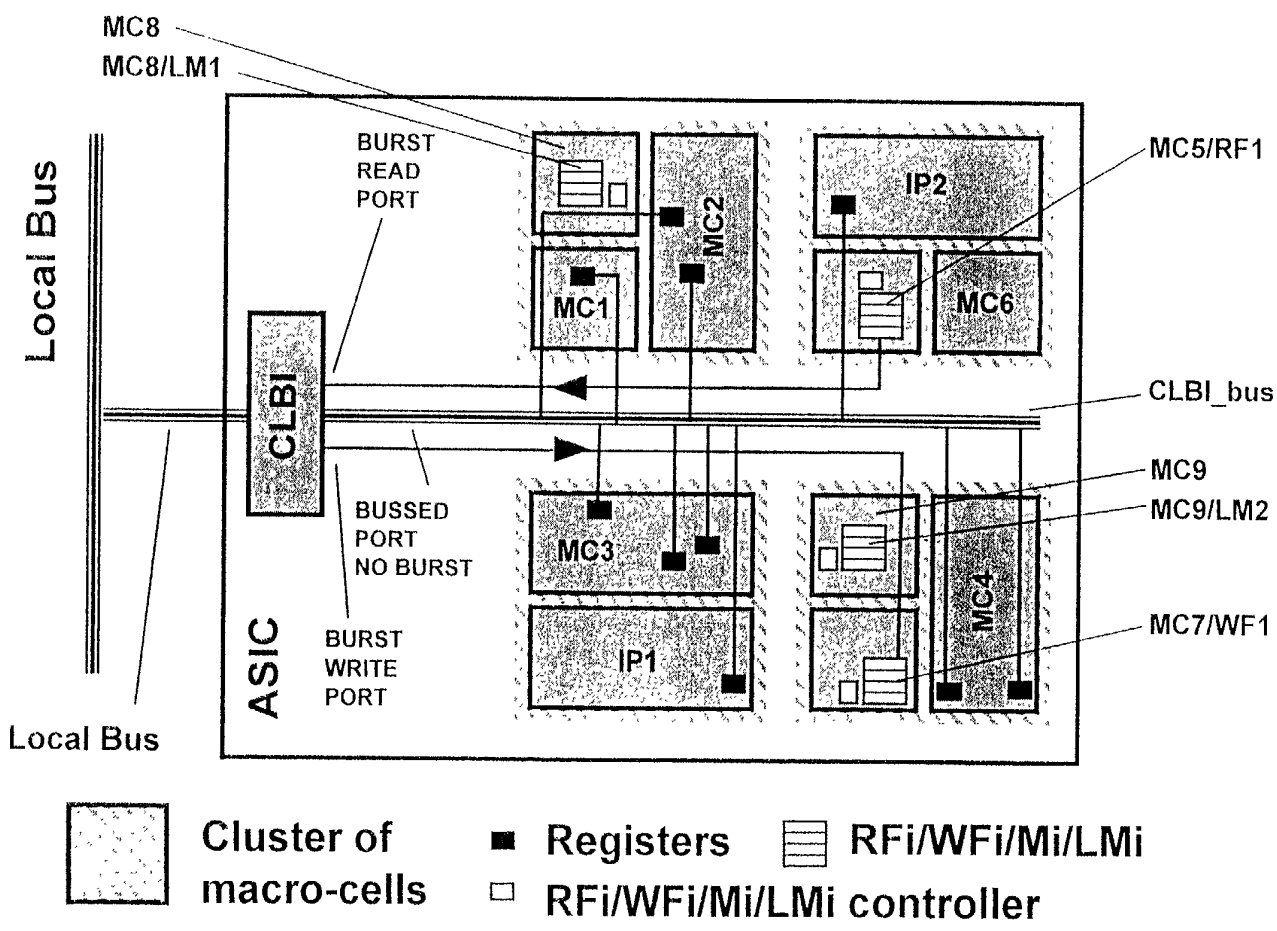
Prior Art

Figure 7



Prior Art

Figure 8



Prior Art

Figure 9

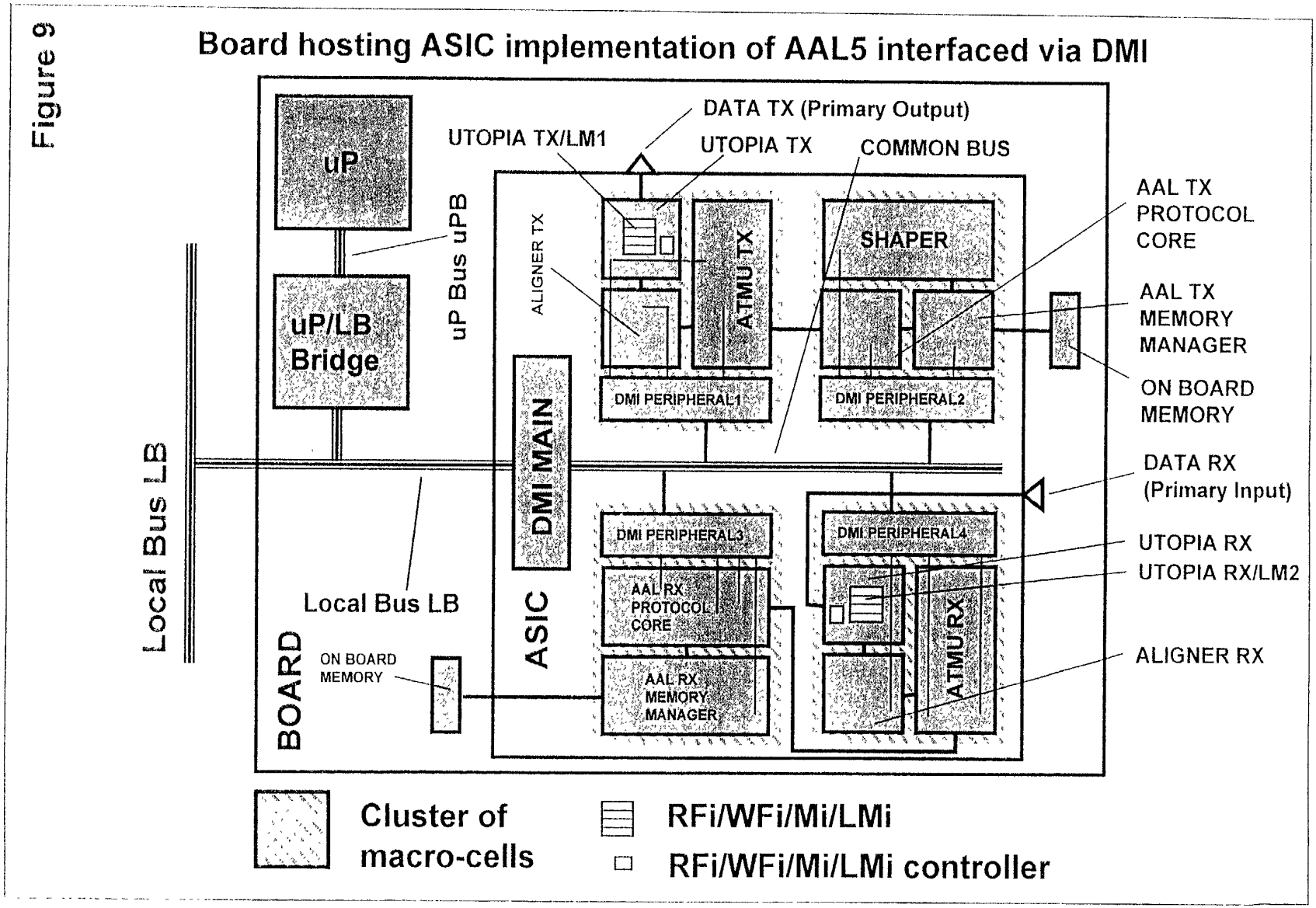
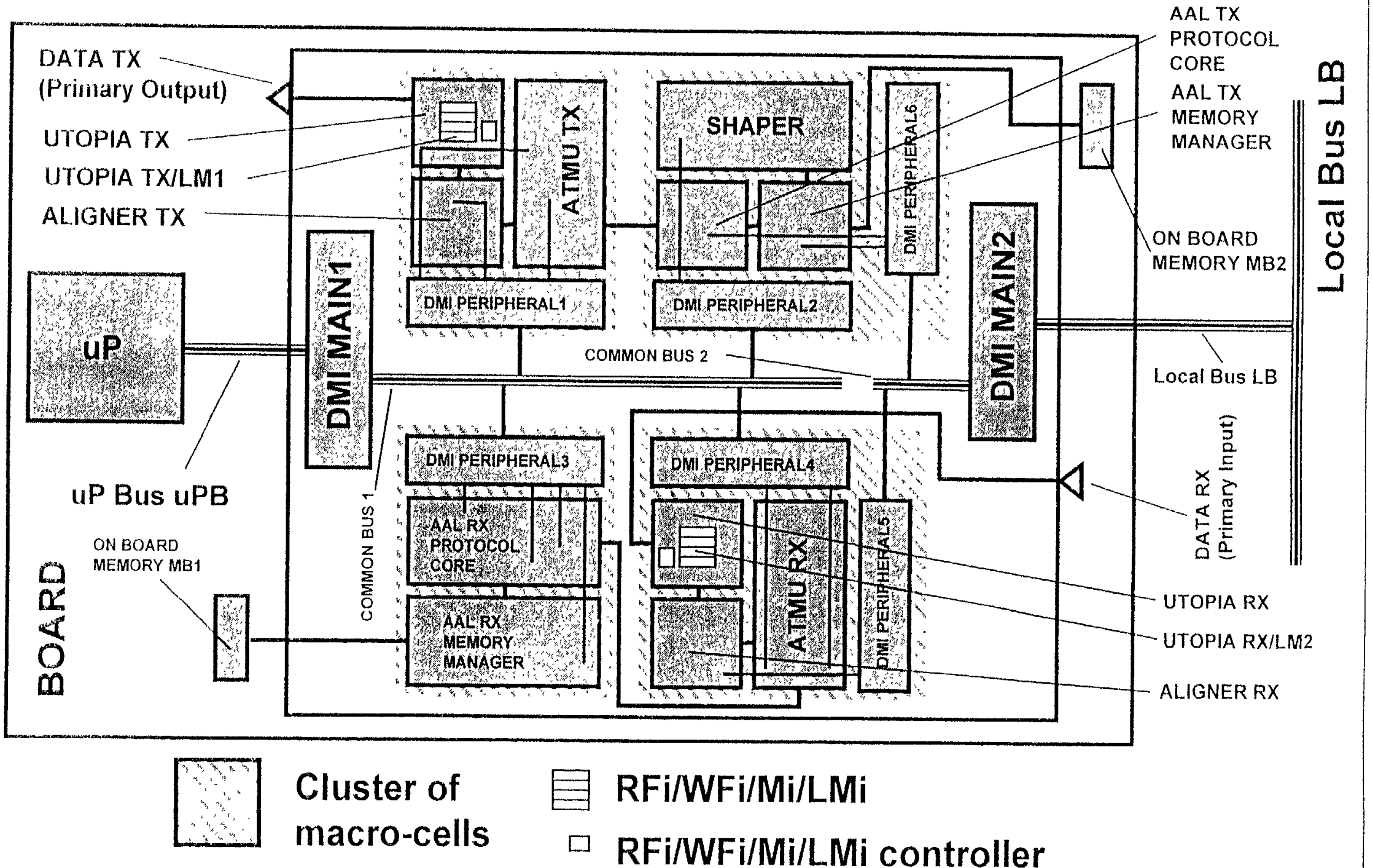

Board hosting ASIC implementation of AAL5 interfaced via DMI
uP
uP/LB Bridge
uP Bus uPB
Local Bus LB
Local Bus LB
BOARD
ON BOARD MEMORY
ASIC
DMI MAIN
ALIGNER TX
ATMU TX
SHAPER
DMI PERIPHERAL1
DMI PERIPHERAL2
DMI PERIPHERAL3
DMI PERIPHERAL4
AAL RX PROTOCOL CORE
AAL RX MEMORY MANAGER
ATMU RX
UTOPIA TX/LM1
DATA TX (Primary Output)
UTOPIA TX
COMMON BUS
AAL TX PROTOCOL CORE
AAL TX MEMORY MANAGER
ON BOARD MEMORY
DATA RX (Primary Input)
UTOPIA RX
UTOPIA RX/LM2
ALIGNER RX
Cluster of macro-cells
RFi/WFi/Mi/LMi
RFi/WFi/Mi/LMi controller

Figure 10

Board hosting FPGA bread-boarding implementation of a DMI for microprocessor interface and a DMI for local bus interface



DATA TX
(Primary Output)
UTOPIA TX
UTOPIA TX/LM1
ALIGNER TX
uP
uP Bus uPB
ON BOARD
MEMORY MB1
BOARD
DMI MAIN1
COMMON BUS 1
ATMU TX
DMI PERIPHERAL1
SHAPER
DMI PERIPHERAL2
DMI PERIPHERAL6
COMMON BUS 2
DMI PERIPHERAL3
AAL RX
PROTOCOL
CORE
AAL RX
MEMORY
MANAGER
DMI PERIPHERAL4
ATMU RX
DMI PERIPHERAL5
DMI MAIN2
AAL TX
PROTOCOL
CORE
AAL TX
MEMORY
MANAGER
ON BOARD
MEMORY MB2
Local Bus LB
Local Bus LB
DATA RX
(Primary Input)
UTOPIA RX
UTOPIA RX/LM2
ALIGNER RX
Cluster of
macro-cells
RFi/WFi/Mi/LMi
RFi/WFi/Mi/LMi controller

Figure 11

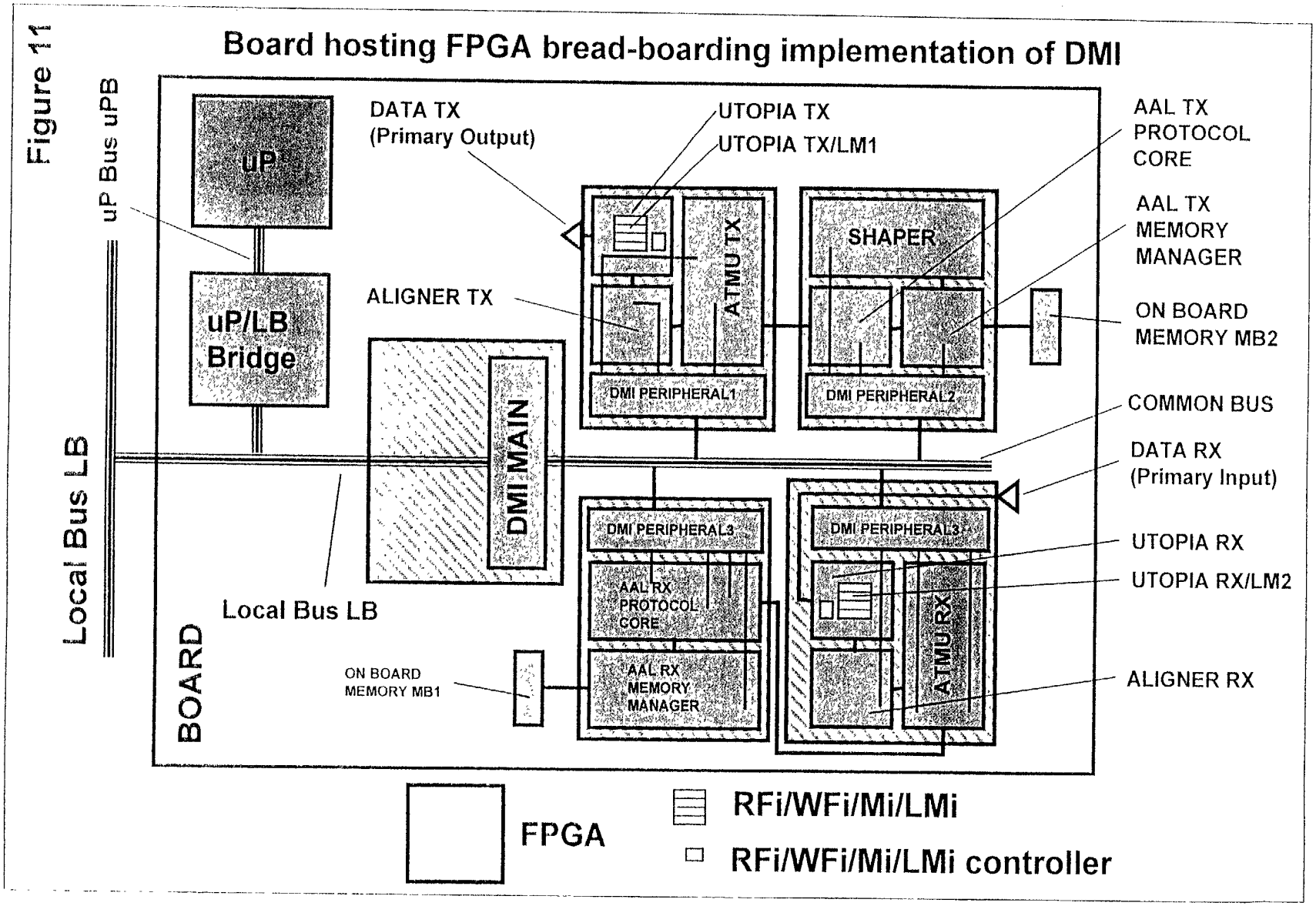

Board hosting FPGA bread-boarding implementation of DMI
uP
uP Bus uPB
uP/LB Bridge
Local Bus LB
BOARD
DATA TX
(Primary Output)
UTOPIA TX
UTOPIA TX/LM1
ATMU TX
SHAPER
AAL TX PROTOCOL CORE
AAL TX MEMORY MANAGER
ON BOARD MEMORY MB2
ALIGNER TX
DMI MAIN
DMI PERIPHERAL1
DMI PERIPHERAL2
COMMON BUS
DATA RX
(Primary Input)
Local Bus LB
DMI PERIPHERAL3
DMI PERIPHERAL3
UTOPIA RX
UTOPIA RX/LM2
AAL RX PROTOCOL CORE
ATMU RX
ON BOARD MEMORY MB1
AAL RX MEMORY MANAGER
ALIGNER RX
FPGA
RFi/WFi/Mi/LMi
RFi/WFi/Mi/LMi controller

Figure 12

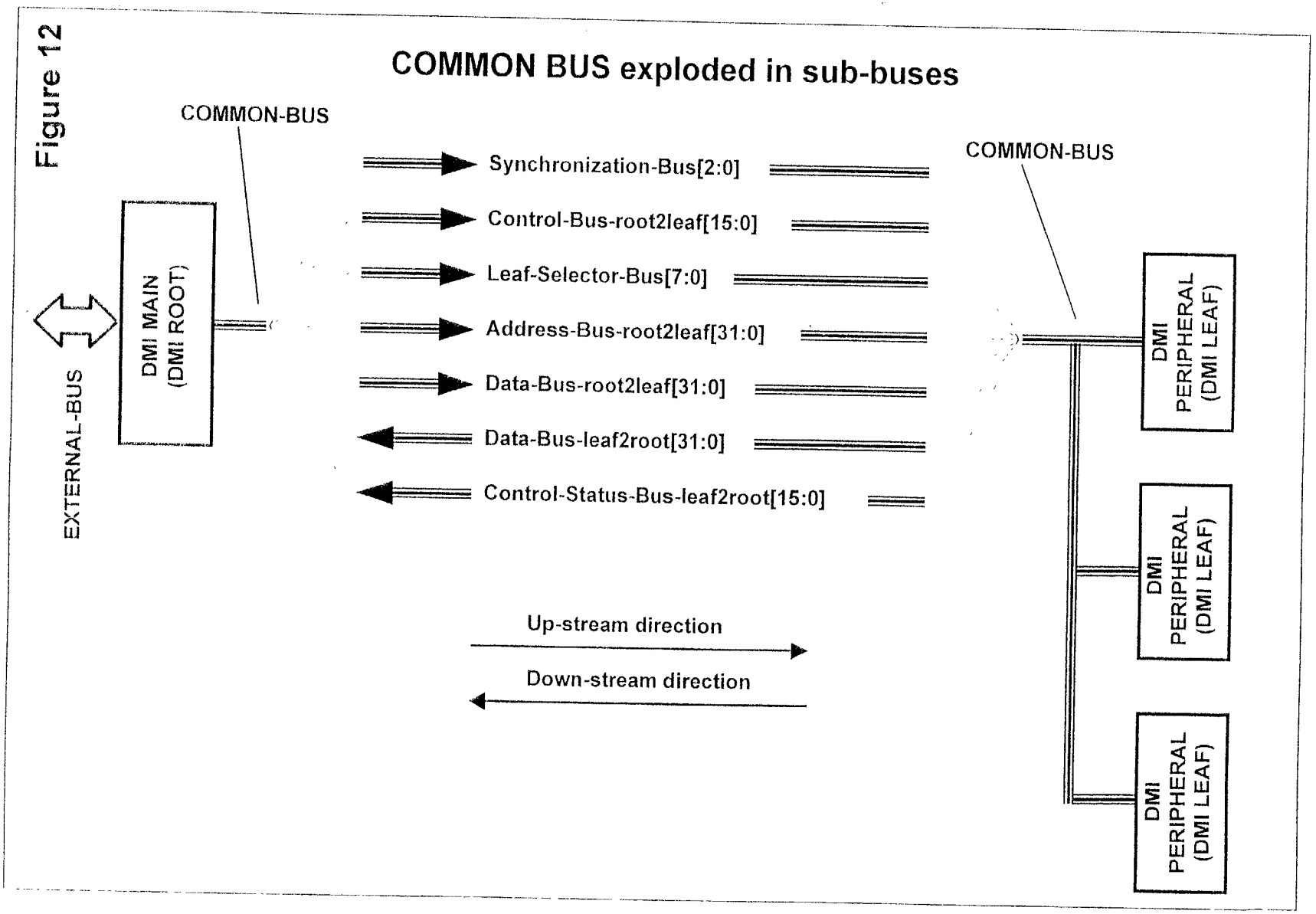
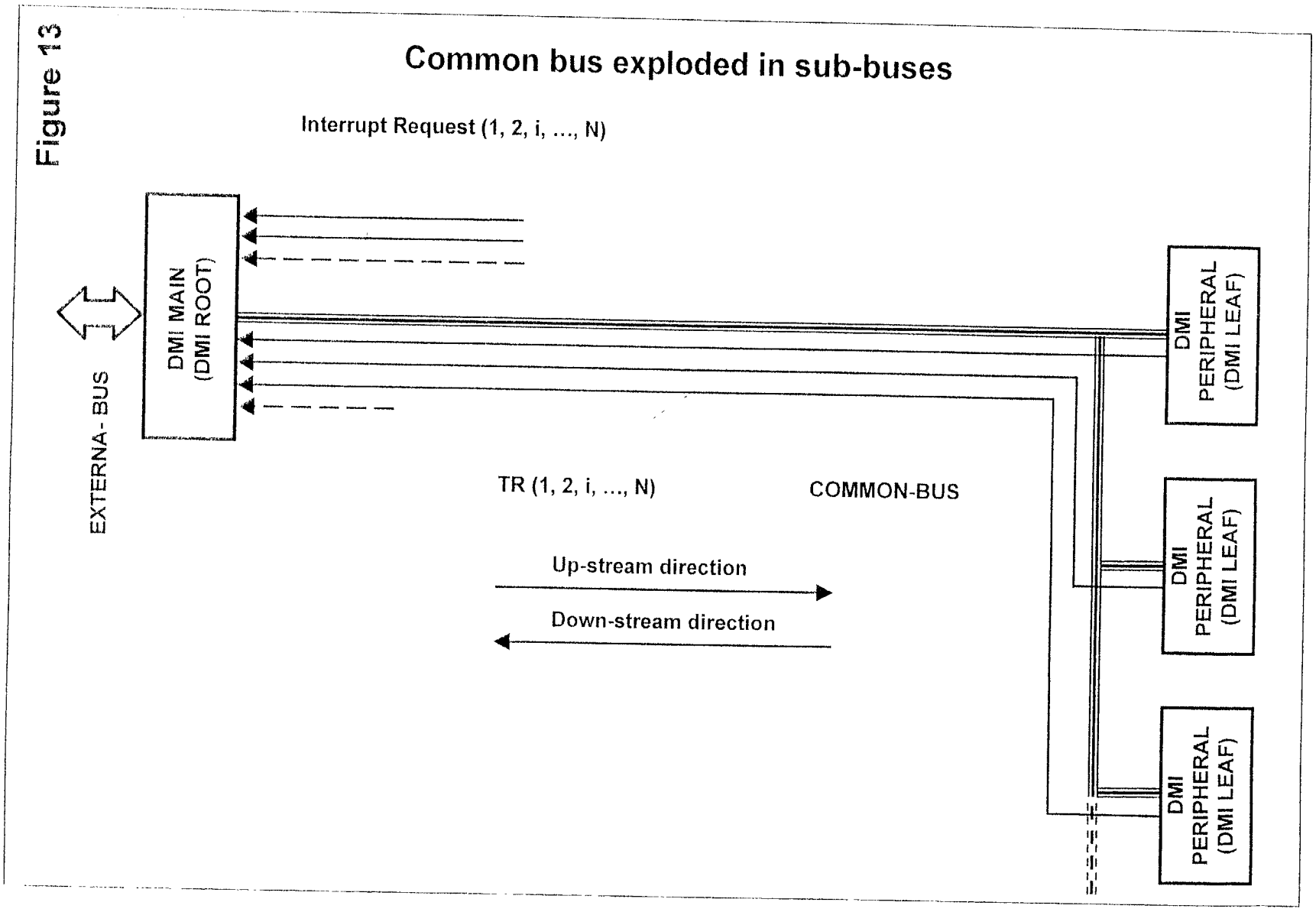

COMMON BUS exploded in sub-buses
COMMON-BUS
EXTERNAL-BUS
DMI MAIN (DMI ROOT)
Synchronization-Bus[2:0]
Control-Bus-root2leaf[15:0]
Leaf-Selector-Bus[7:0]
Address-Bus-root2leaf[31:0]
Data-Bus-root2leaf[31:0]
Data-Bus-leaf2root[31:0]
Control-Status-Bus-leaf2root[15:0]
COMMON-BUS
DMI PERIPHERAL (DMI LEAF)
DMI PERIPHERAL (DMI LEAF)
DMI PERIPHERAL (DMI LEAF)
Up-stream direction
Down-stream direction

Figure 13


Common bus exploded in sub-buses
Interrupt Request (1, 2, i, ..., N)
DMI MAIN (DMI ROOT)
EXTERNA- BUS
DMI PERIPHERAL (DMI LEAF)
DMI PERIPHERAL (DMI LEAF)
DMI PERIPHERAL (DMI LEAF)
TR (1, 2, i, ..., N)
COMMON-BUS
Up-stream direction
Down-stream direction

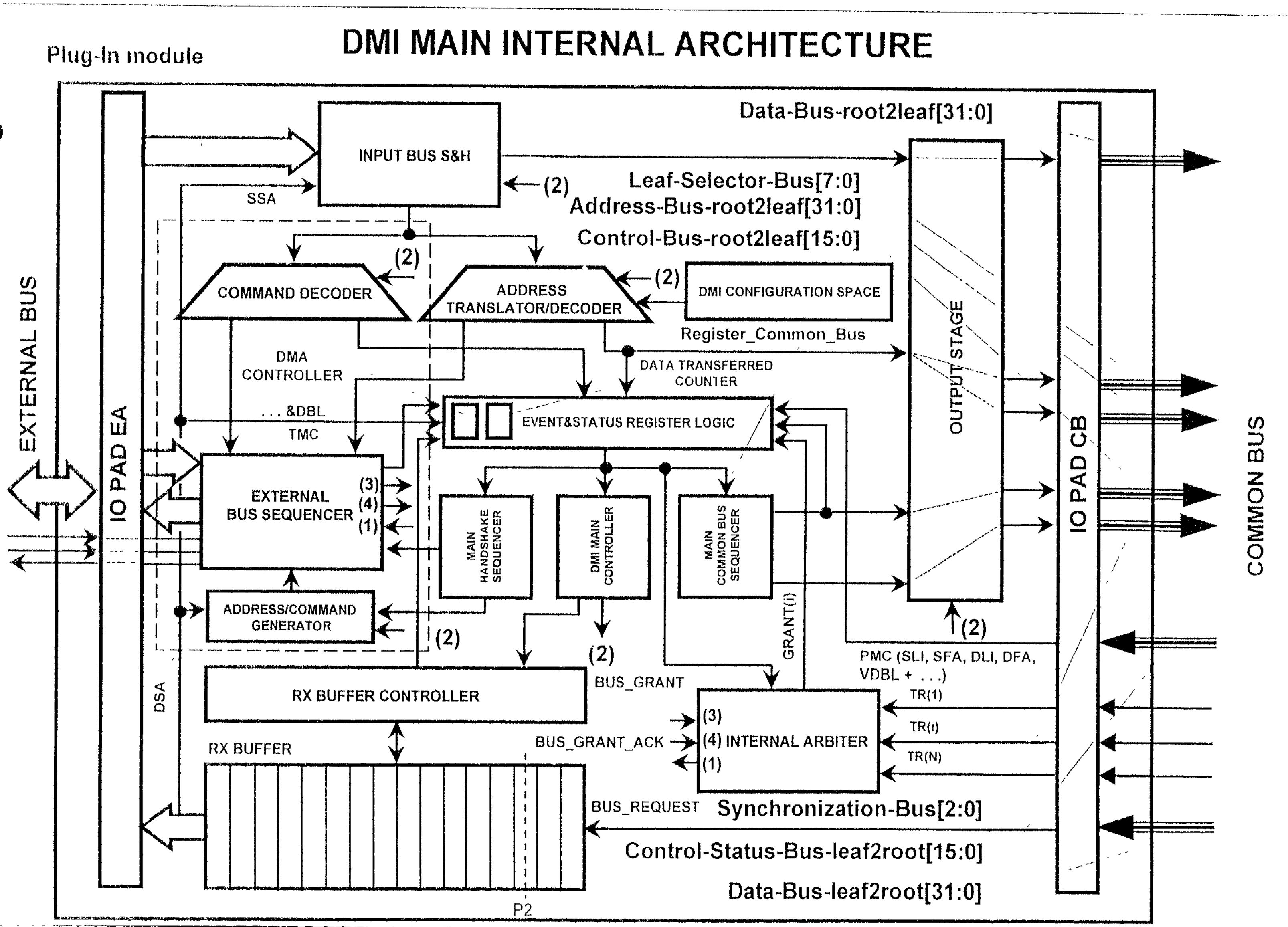

DMI MAIN INTERNAL ARCHITECTURE
Plug-In module
EXTERNAL BUS
EB_GRANT
EB_GRANT_ACK
EB_REQUEST
IO PAD EA
INPUT BUS S&H
SSA
(2)
COMMAND DECODER
ADDRESS TRANSLATOR/DECODER
DMI CONFIGURATION SPACE
Register_Common_Bus
DATA TRANSFERRED COUNTER
DMA CONTROLLER
. . . &DBL
TMC
EVENT&STATUS REGISTER LOGIC
EXTERNAL BUS SEQUENCER
(3)
(4)
(1)
MAIN HANDSHAKE SEQUENCER
DMI MAIN CONTROLLER
MAIN COMMON BUS SEQUENCER
ADDRESS/COMMAND GENERATOR
RX BUFFER CONTROLLER
RX BUFFER
DSA
P2
BUS_GRANT
BUS_GRANT_ACK
BUS_REQUEST
GRANT(i)
INTERNAL ARBITER
OUTPUT STAGE
IO PAD CB
COMMON BUS
Data-Bus-root2leaf[31:0]
Leaf-Selector-Bus[7:0]
Address-Bus-root2leaf[31:0]
Control-Bus-root2leaf[15:0]
PMC (SLI, SFA, DLI, DFA, VDBL + . . .)
TR(1)
TR(i)
TR(N)
Synchronization-Bus[2:0]
Control-Status-Bus-leaf2root[15:0]
Data-Bus-leaf2root[31:0]

Figure 14

Figure 15

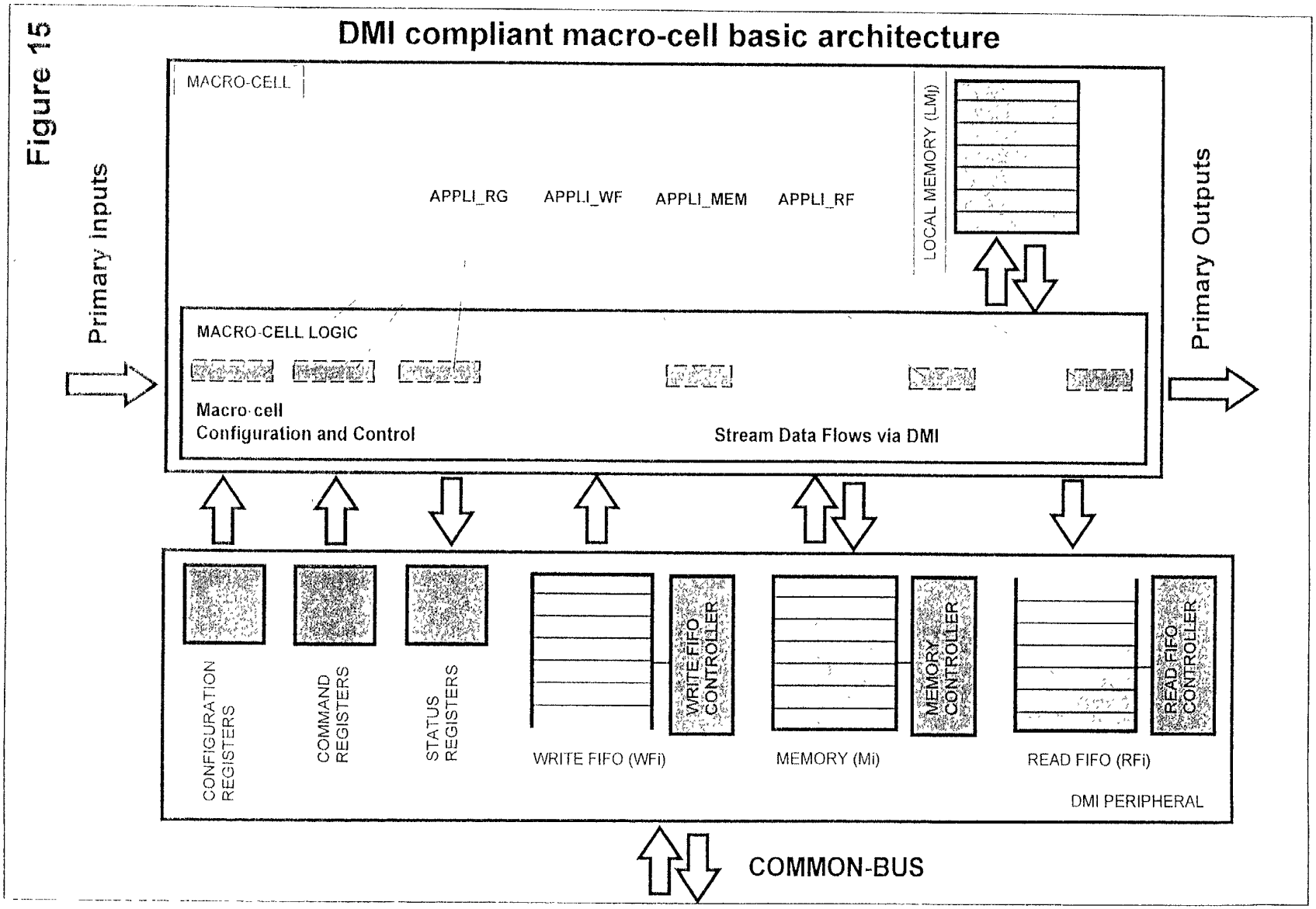

DMI compliant macro-cell basic architecture
MACRO-CELL
LOCAL MEMORY (LMj)
APPLI_RG
APPLI_WF
APPLI_MEM
APPLI_RF
Primary Inputs
Primary Outputs
MACRO-CELL LOGIC
Macro-cell
Configuration and Control
Stream Data Flows via DMI
CONFIGURATION REGISTERS
COMMAND REGISTERS
STATUS REGISTERS
WRITE FIFO CONTROLLER
MEMORY CONTROLLER
READ FIFO CONTROLLER
WRITE FIFO (WFi)
MEMORY (Mi)
READ FIFO (RFi)
DMI PERIPHERAL
COMMON-BUS

Figure 16

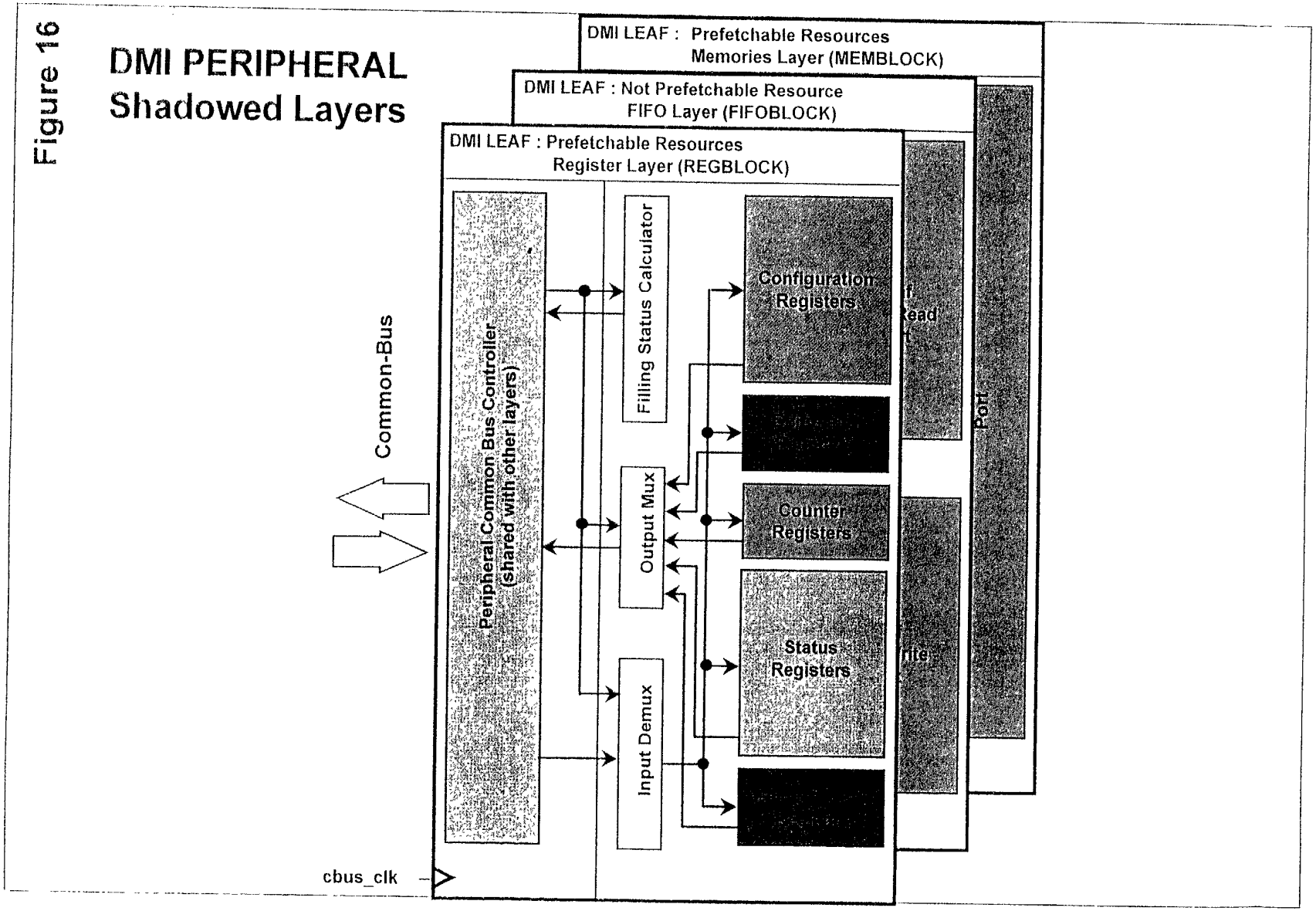

DMI PERIPHERAL
Shadowed Layers
DMI LEAF : Prefetchable Resources
Memories Layer (MEMBLOCK)
DMI LEAF : Not Prefetchable Resource
FIFO Layer (FIFOBLOCK)
DMI LEAF : Prefetchable Resources
Register Layer (REGBLOCK)
Common-Bus
Peripheral Common Bus Controller
(shared with other layers)
Filling Status Calculator
Output Mux
Input Demux
Configuration Registers
Counter Registers
Status Registers
cbus_clk

Figure 17

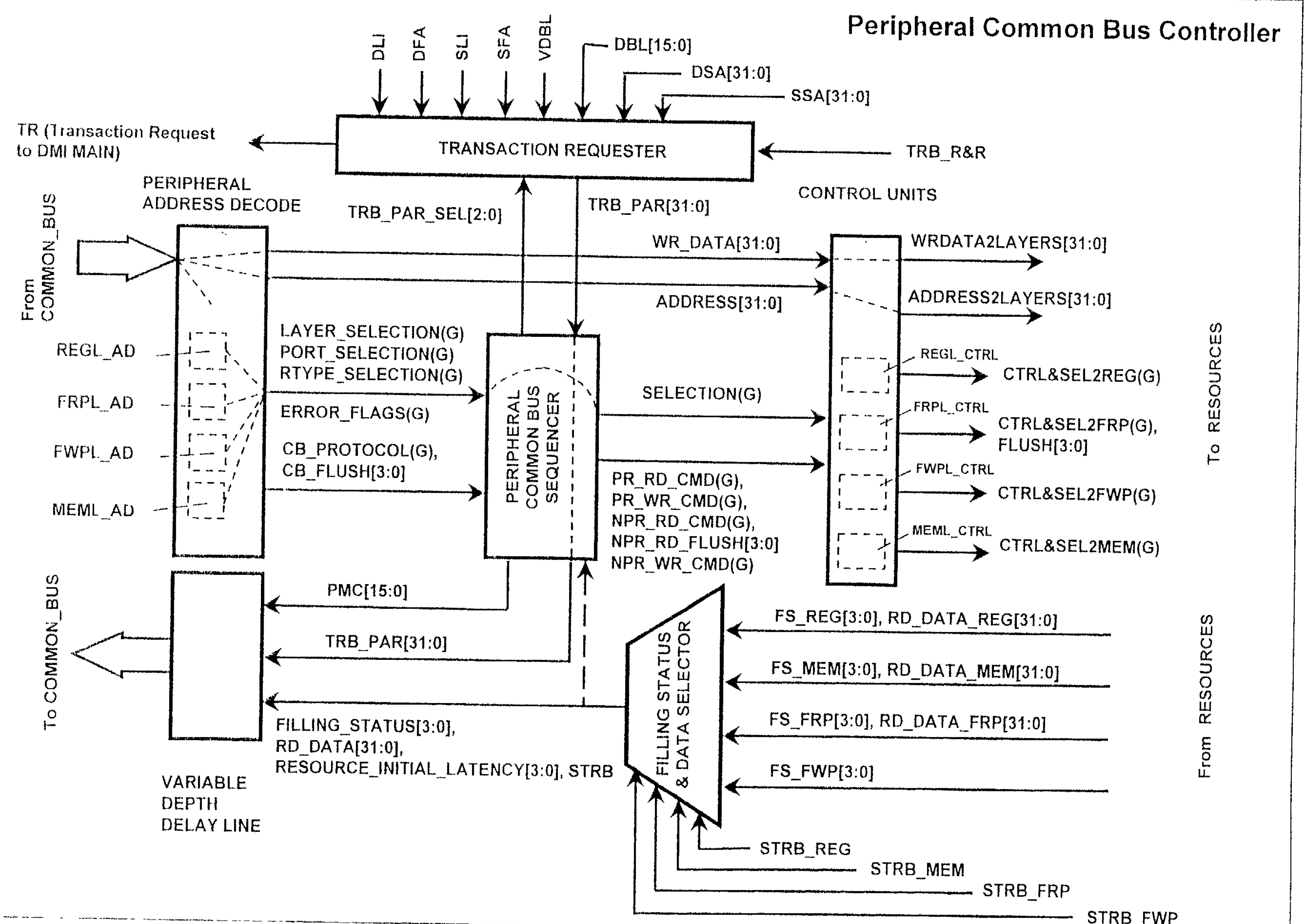

Peripheral Common Bus Controller
DLI
DFA
SLI
SFA
VDBL
DBL[15:0]
DSA[31:0]
SSA[31:0]
TR (Transaction Request to DMI MAIN)
TRANSACTION REQUESTER
TRB_R&R
PERIPHERAL ADDRESS DECODE
CONTROL UNITS
TRB_PAR_SEL[2:0]
TRB_PAR[31:0]
From COMMON_BUS
WR_DATA[31:0]
WRDATA2LAYERS[31:0]
ADDRESS[31:0]
ADDRESS2LAYERS[31:0]
REGL_AD
FRPL_AD
FWPL_AD
MEML_AD
LAYER_SELECTION(G)
PORT_SELECTION(G)
RTYPE_SELECTION(G)
ERROR_FLAGS(G)
CB_PROTOCOL(G),
CB_FLUSH[3:0]
PERIPHERAL COMMON BUS SEQUENCER
SELECTION(G)
PR_RD_CMD(G),
PR_WR_CMD(G),
NPR_RD_CMD(G),
NPR_RD_FLUSH[3:0]
NPR_WR_CMD(G)
REGL_CTRL
CTRL&SEL2REG(G)
FRPL_CTRL
CTRL&SEL2FRP(G),
FLUSH[3:0]
FWPL_CTRL
CTRL&SEL2FWP(G)
MEML_CTRL
CTRL&SEL2MEM(G)
To RESOURCES
To COMMON_BUS
PMC[15:0]
TRB_PAR[31:0]
FILLING_STATUS[3:0],
RD_DATA[31:0],
RESOURCE_INITIAL_LATENCY[3:0], STRB
VARIABLE DEPTH DELAY LINE
FILLING STATUS & DATA SELECTOR
FS_REG[3:0], RD_DATA_REG[31:0]
FS_MEM[3:0], RD_DATA_MEM[31:0]
FS_FRP[3:0], RD_DATA_FRP[31:0]
FS_FWP[3:0]
From RESOURCES
STRB_REG
STRB_MEM
STRB_FRP
STRB_FWP

Figure 18

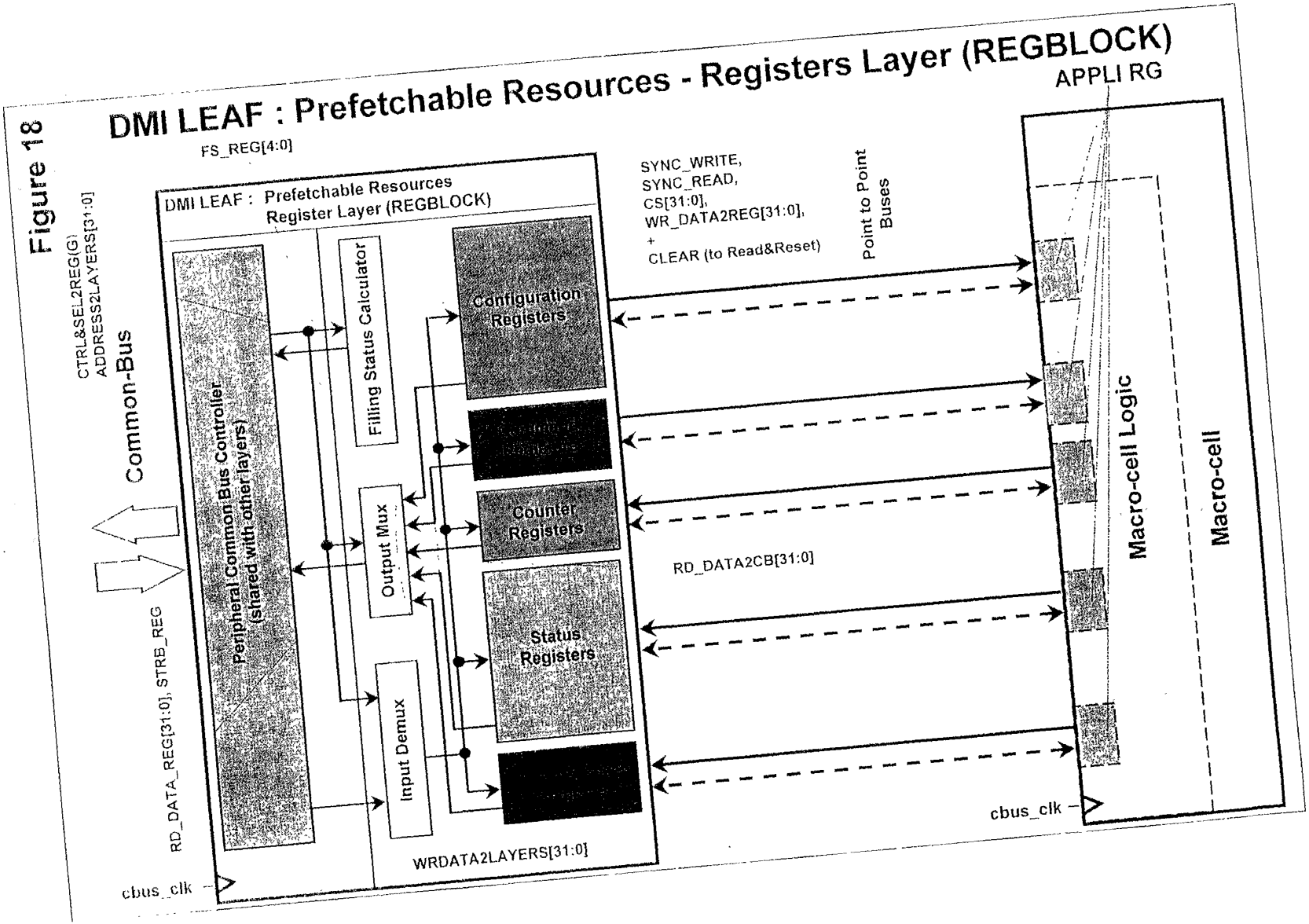


Figure 19

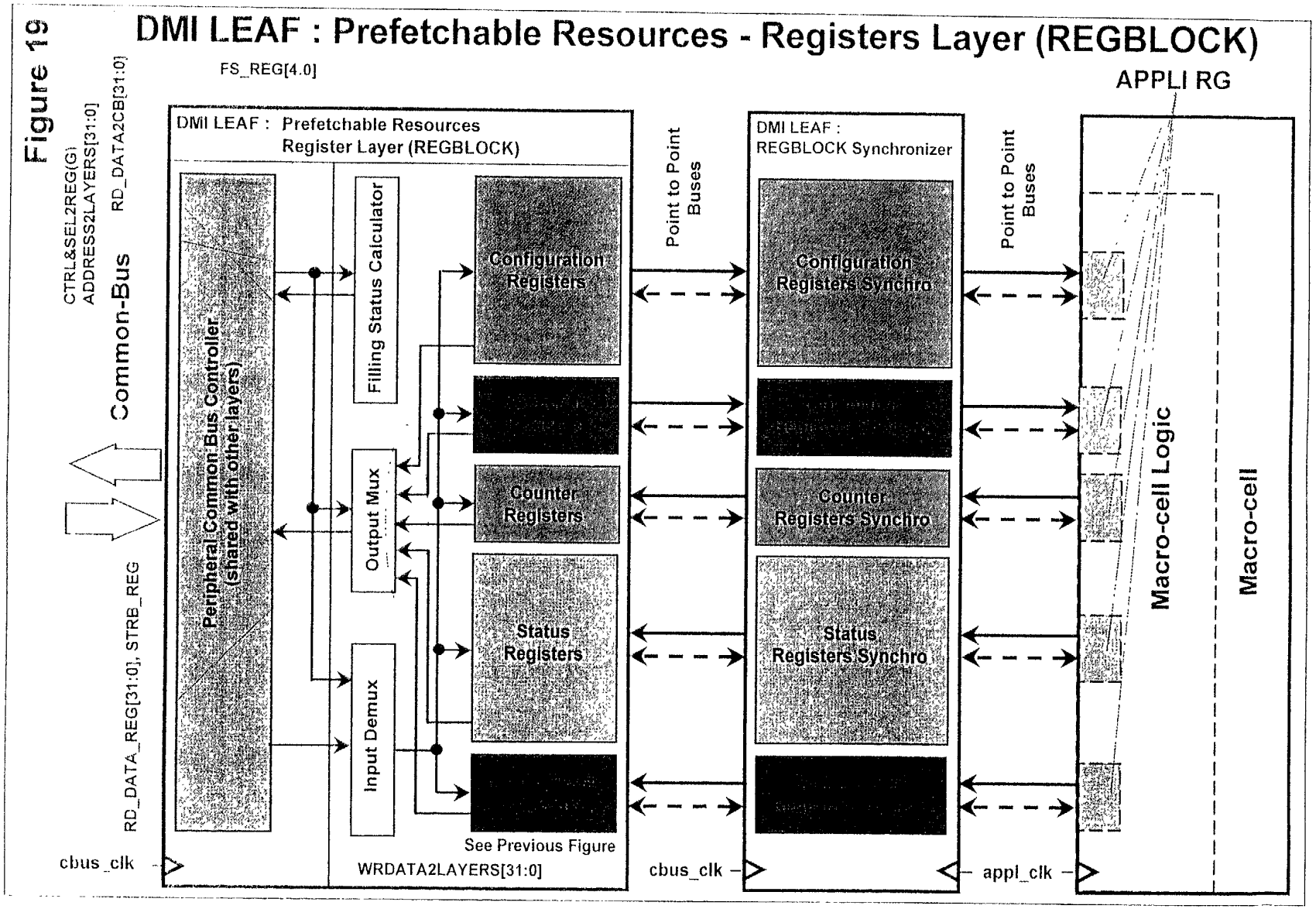

DMI LEAF : Prefetchable Resources - Registers Layer (REGBLOCK)
FS_REG[4.0]
APPLI RG
DMI LEAF : Prefetchable Resources
Register Layer (REGBLOCK)
DMI LEAF :
REGBLOCK Synchronizer
Point to Point Buses
Point to Point Buses
CTRL&SEL2REG(G)
ADDRESS2LAYERS[31:0]
Common-Bus
RD_DATA2CB[31:0]
Peripheral Common Bus Controller (shared with other layers)
Filling Status Calculator
Output Mux
Input Demux
Configuration Registers
Counter Registers
Status Registers
Configuration Registers Synchro
Counter Registers Synchro
Status Registers Synchro
Macro-cell Logic
Macro-cell
RD_DATA_REG[31:0], STRB_REG
See Previous Figure
WRDATA2LAYERS[31:0]
cbus_clk
cbus_clk
appl_clk

Figure 20

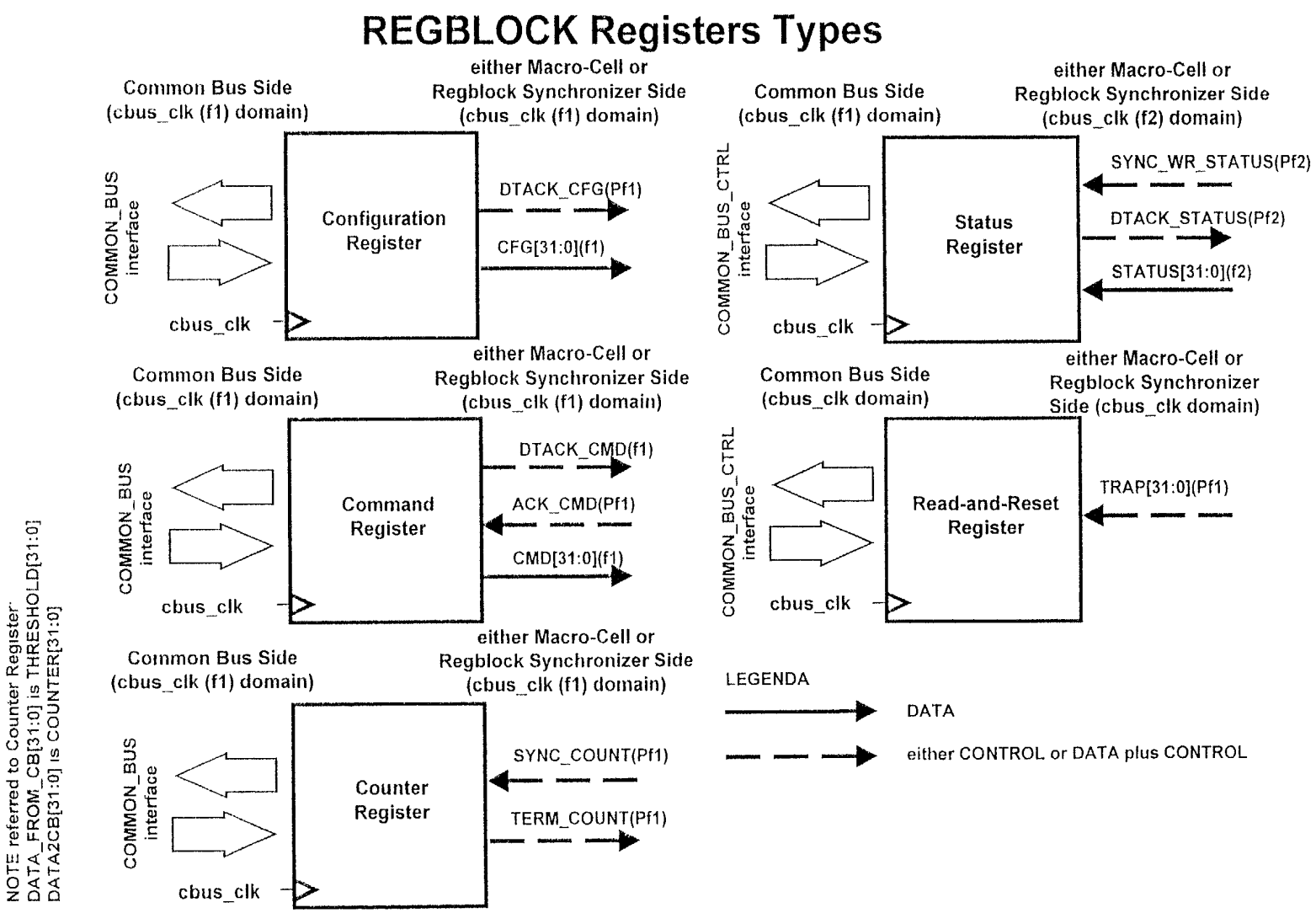

REGBLOCK Registers Types
Common Bus Side
(cbus_clk (f1) domain)
either Macro-Cell or
Regblock Synchronizer Side
(cbus_clk (f1) domain)
COMMON_BUS
interface
Configuration
Register
DTACK_CFG(Pf1)
CFG[31:0](f1)
cbus_clk
Common Bus Side
(cbus_clk (f1) domain)
either Macro-Cell or
Regblock Synchronizer Side
(cbus_clk (f2) domain)
COMMON_BUS_CTRL
interface
Status
Register
SYNC_WR_STATUS(Pf2)
DTACK_STATUS(Pf2)
STATUS[31:0](f2)
cbus_clk
Common Bus Side
(cbus_clk (f1) domain)
either Macro-Cell or
Regblock Synchronizer Side
(cbus_clk (f1) domain)
COMMON_BUS
interface
Command
Register
DTACK_CMD(f1)
ACK_CMD(Pf1)
CMD[31:0](f1)
cbus_clk
Common Bus Side
(cbus_clk domain)
either Macro-Cell or
Regblock Synchronizer
Side (cbus_clk domain)
COMMON_BUS_CTRL
interface
Read-and-Reset
Register
TRAP[31:0](Pf1)
cbus_clk
Common Bus Side
(cbus_clk (f1) domain)
either Macro-Cell or
Regblock Synchronizer Side
(cbus_clk (f1) domain)
COMMON_BUS
interface
Counter
Register
SYNC_COUNT(Pf1)
TERM_COUNT(Pf1)
cbus_clk
LEGENDA
DATA
either CONTROL or DATA plus CONTROL
NOTE referred to Counter Register:
DATA_FROM_CB[31:0] is THRESHOLD[31:0]
DATA2CB[31:0] is COUNTER[31:0]

Figure 21

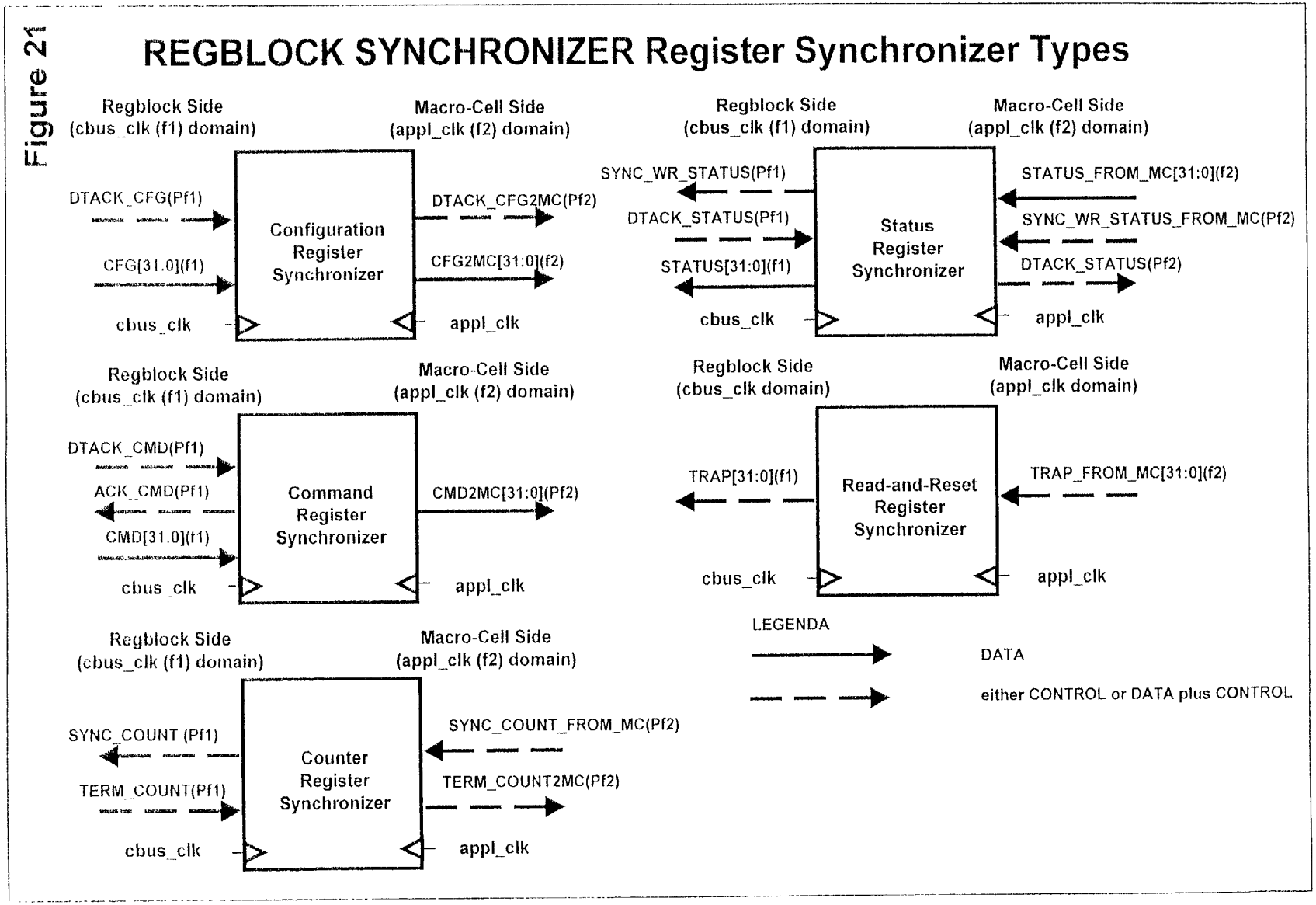

REGBLOCK SYNCHRONIZER Register Synchronizer Types
Regblock Side
(cbus_clk (f1) domain)
Macro-Cell Side
(appl_clk (f2) domain)
DTACK_CFG(Pf1)
CFG[31.0](f1)
cbus_clk
Configuration
Register
Synchronizer
DTACK_CFG2MC(Pf2)
CFG2MC[31:0](f2)
appl_clk
Regblock Side
(cbus_clk (f1) domain)
Macro-Cell Side
(appl_clk (f2) domain)
SYNC_WR_STATUS(Pf1)
DTACK_STATUS(Pf1)
STATUS[31:0](f1)
cbus_clk
Status
Register
Synchronizer
STATUS_FROM_MC[31:0](f2)
SYNC_WR_STATUS_FROM_MC(Pf2)
DTACK_STATUS(Pf2)
appl_clk
Regblock Side
(cbus_clk (f1) domain)
Macro-Cell Side
(appl_clk (f2) domain)
DTACK_CMD(Pf1)
ACK_CMD(Pf1)
CMD[31.0](f1)
cbus_clk
Command
Register
Synchronizer
CMD2MC[31:0](Pf2)
appl_clk
Regblock Side
(cbus_clk domain)
Macro-Cell Side
(appl_clk domain)
TRAP[31:0](f1)
cbus_clk
Read-and-Reset
Register
Synchronizer
TRAP_FROM_MC[31:0](f2)
appl_clk
Regblock Side
(cbus_clk (f1) domain)
Macro-Cell Side
(appl_clk (f2) domain)
SYNC_COUNT (Pf1)
TERM_COUNT(Pf1)
cbus_clk
Counter
Register
Synchronizer
SYNC_COUNT_FROM_MC(Pf2)
TERM_COUNT2MC(Pf2)
appl_clk
LEGENDA
DATA
either CONTROL or DATA plus CONTROL

Figure 22

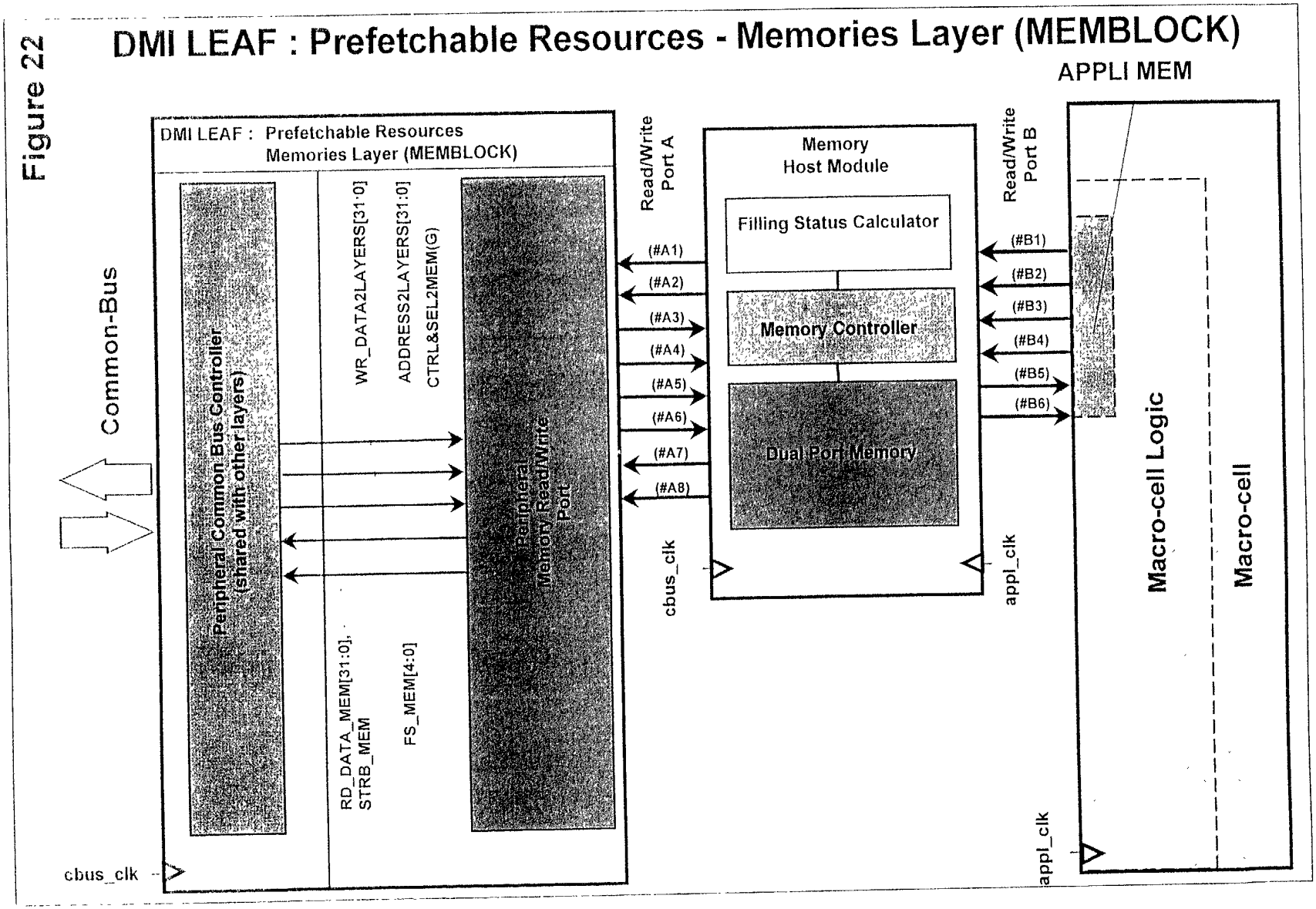

DMI LEAF : Prefetchable Resources - Memories Layer (MEMBLOCK)
APPLI MEM
DMI LEAF : Prefetchable Resources
Memories Layer (MEMBLOCK)
Common-Bus
Peripheral Common Bus Controller
(shared with other layers)
WR_DATA2LAYERS[31:0]
ADDRESS2LAYERS[31:0]
CTRL&SEL2MEM(G)
RD_DATA_MEM[31:0],
STRB_MEM
FS_MEM[4:0]
Peripheral
Memory Read/Write
Port
cbus_clk
Read/Write
Port A
(#A1)
(#A2)
(#A3)
(#A4)
(#A5)
(#A6)
(#A7)
(#A8)
Memory
Host Module
Filling Status Calculator
Memory Controller
Dual Port Memory
cbus_clk
Read/Write
Port B
(#B1)
(#B2)
(#B3)
(#B4)
(#B5)
(#B6)
appl_clk
appl_clk
Macro-cell Logic
Macro-cell

Figure 23

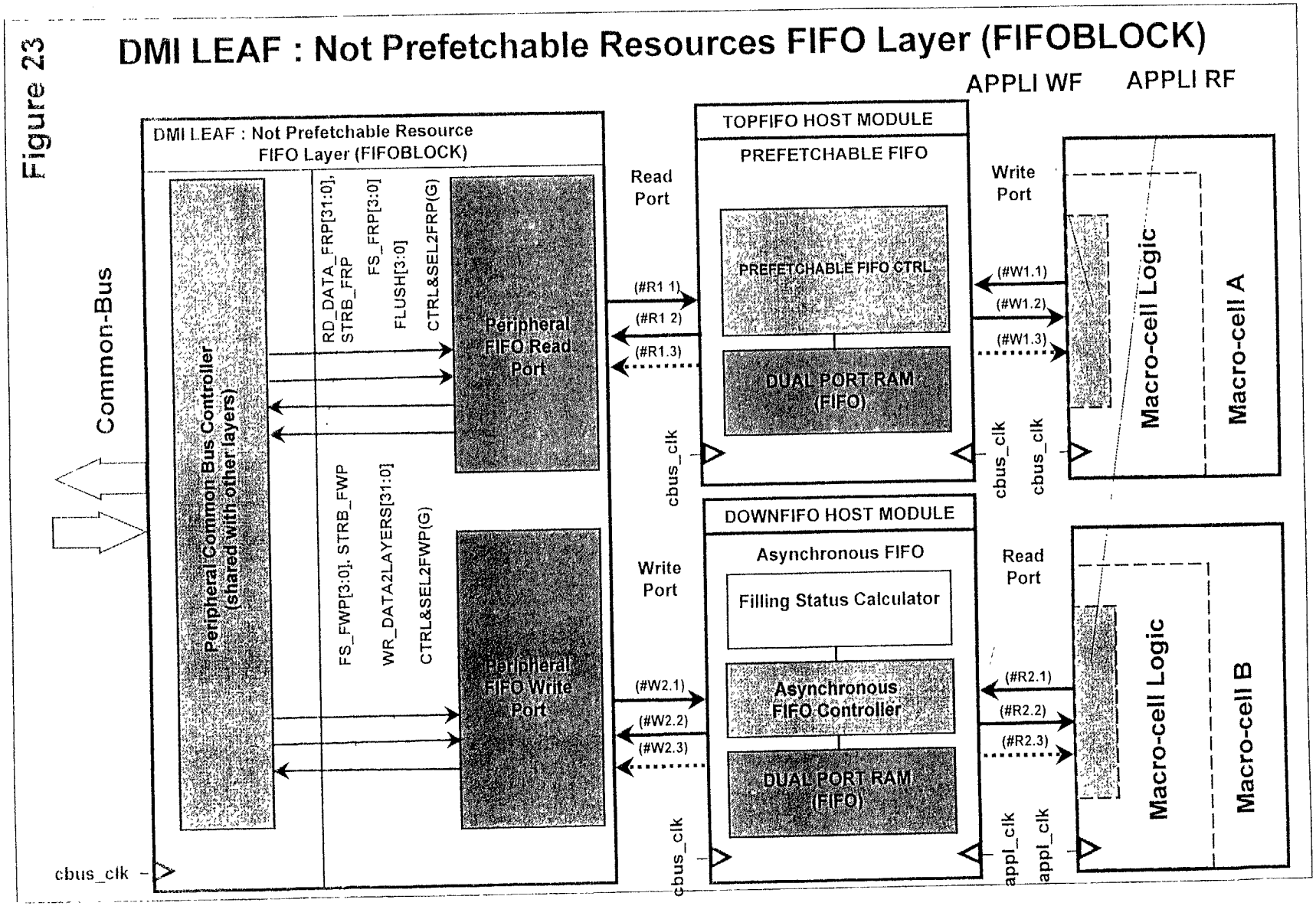

DMI LEAF : Not Prefetchable Resources FIFO Layer (FIFOBLOCK)
APPLI WF
APPLI RF
DMI LEAF : Not Prefetchable Resource FIFO Layer (FIFOBLOCK)
Common-Bus
Peripheral Common Bus Controller (shared with other layers)
RD_DATA_FRP[31:0], STRB_FRP
FS_FRP[3:0]
FLUSH[3:0]
CTRL&SEL2FRP(G)
Peripheral FIFO Read Port
FS_FWP[3:0], STRB_FWP
WR_DATA2LAYERS[31:0]
CTRL&SEL2FWP(G)
Peripheral FIFO Write Port
cbus_clk
Read Port
(#R1.1)
(#R1.2)
(#R1.3)
TOPFIFO HOST MODULE
PREFETCHABLE FIFO
PREFETCHABLE FIFO CTRL
DUAL PORT RAM (FIFO)
Write Port
(#W1.1)
(#W1.2)
(#W1.3)
Macro-cell Logic
Macro-cell A
Write Port
(#W2.1)
(#W2.2)
(#W2.3)
DOWNFIFO HOST MODULE
Asynchronous FIFO
Filling Status Calculator
Asynchronous FIFO Controller
DUAL PORT RAM (FIFO)
Read Port
(#R2.1)
(#R2.2)
(#R2.3)
Macro-cell Logic
Macro-cell B
appl_clk

Figure 24

Command Register and Command Register Synchronizer

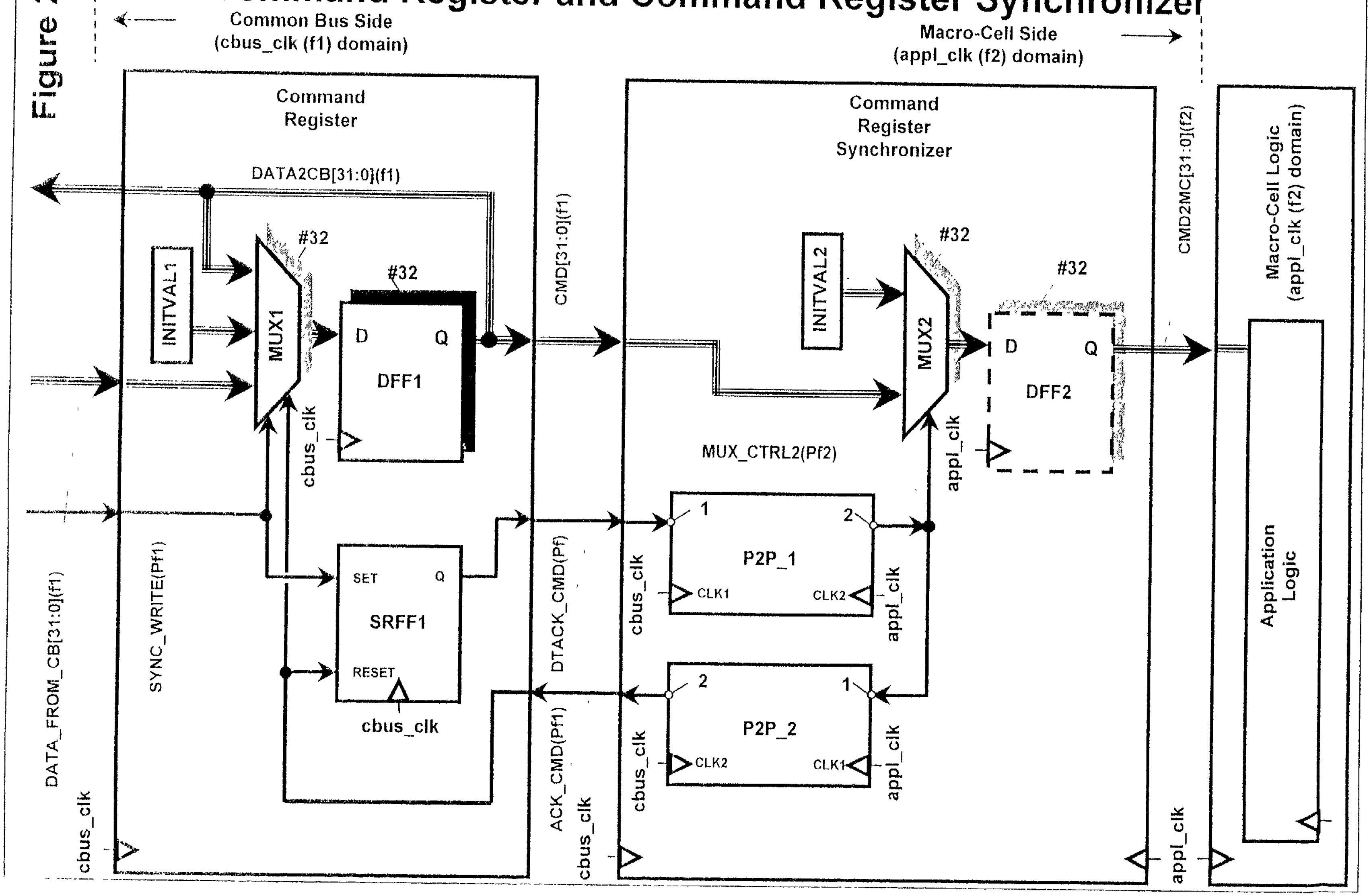

Common Bus Side
(cbus_clk (f1) domain)
Macro-Cell Side
(appl_clk (f2) domain)
Command
Register
DATA2CB[31:0](f1)
INITVAL1
MUX1
#32
#32
D
Q
DFF1
cbus_clk
SET
Q
SRFF1
RESET
cbus_clk
DATA_FROM_CB[31:0](f1)
SYNC_WRITE(Pf1)
cbus_clk
CMD[31:0](f1)
DTACK_CMD(Pf)
ACK_CMD(Pf1)
cbus_clk
Command
Register
Synchronizer
INITVAL2
MUX2
#32
#32
D
Q
DFF2
appl_clk
MUX_CTRL2(Pf2)
1
2
P2P_1
CLK1
CLK2
cbus_clk
appl_clk
2
1
P2P_2
CLK2
CLK1
cbus_clk
appl_clk
CMD2MC[31:0](f2)
Macro-Cell Logic
(appl_clk (f2) domain)
Application
Logic
appl_clk

Figure 25

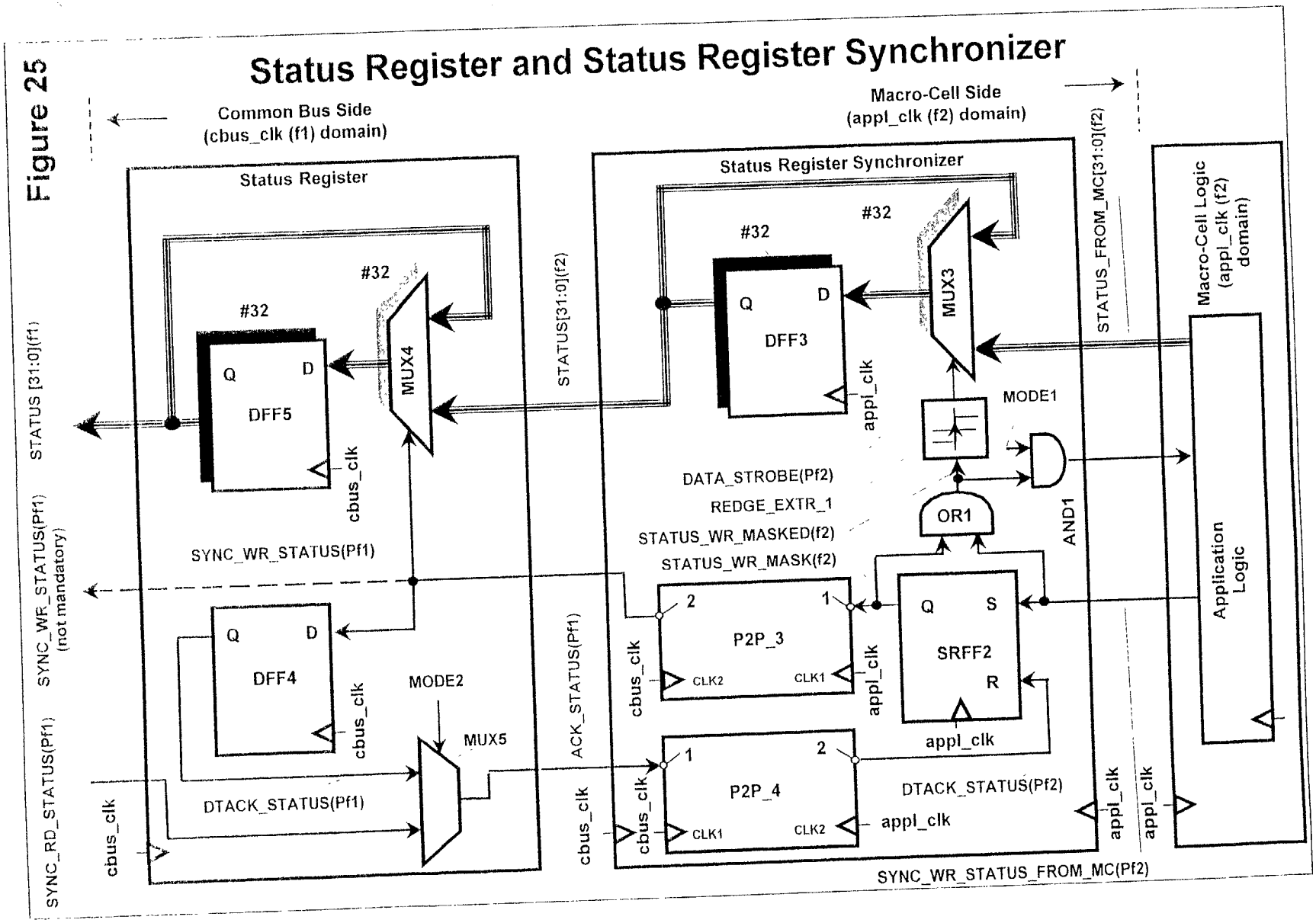

Status Register and Status Register Synchronizer
Common Bus Side
(cbus_clk (f1) domain)
Macro-Cell Side
(appl_clk (f2) domain)
Status Register
Status Register Synchronizer
#32
DFF5
DFF4
DFF3
MUX4
MUX5
MUX3
Q
D
cbus_clk
appl_clk
STATUS [31:0](f1)
STATUS[31:0](f2)
STATUS_FROM_MC[31:0](f2)
SYNC_WR_STATUS(Pf1)
(not mandatory)
SYNC_WR_STATUS(Pf1)
SYNC_RD_STATUS(Pf1)
DTACK_STATUS(Pf1)
MODE2
MODE1
DATA_STROBE(Pf2)
REDGE_EXTR_1
STATUS_WR_MASKED(f2)
STATUS_WR_MASK(f2)
OR1
AND1
P2P_3
P2P_4
CLK1
CLK2
SRFF2
S
R
ACK_STATUS(Pf1)
DTACK_STATUS(Pf2)
SYNC_WR_STATUS_FROM_MC(Pf2)
Macro-Cell Logic
(appl_clk (f2)
domain)
Application
Logic

Figure 26

Pulse to Pulse Synchronization Unit

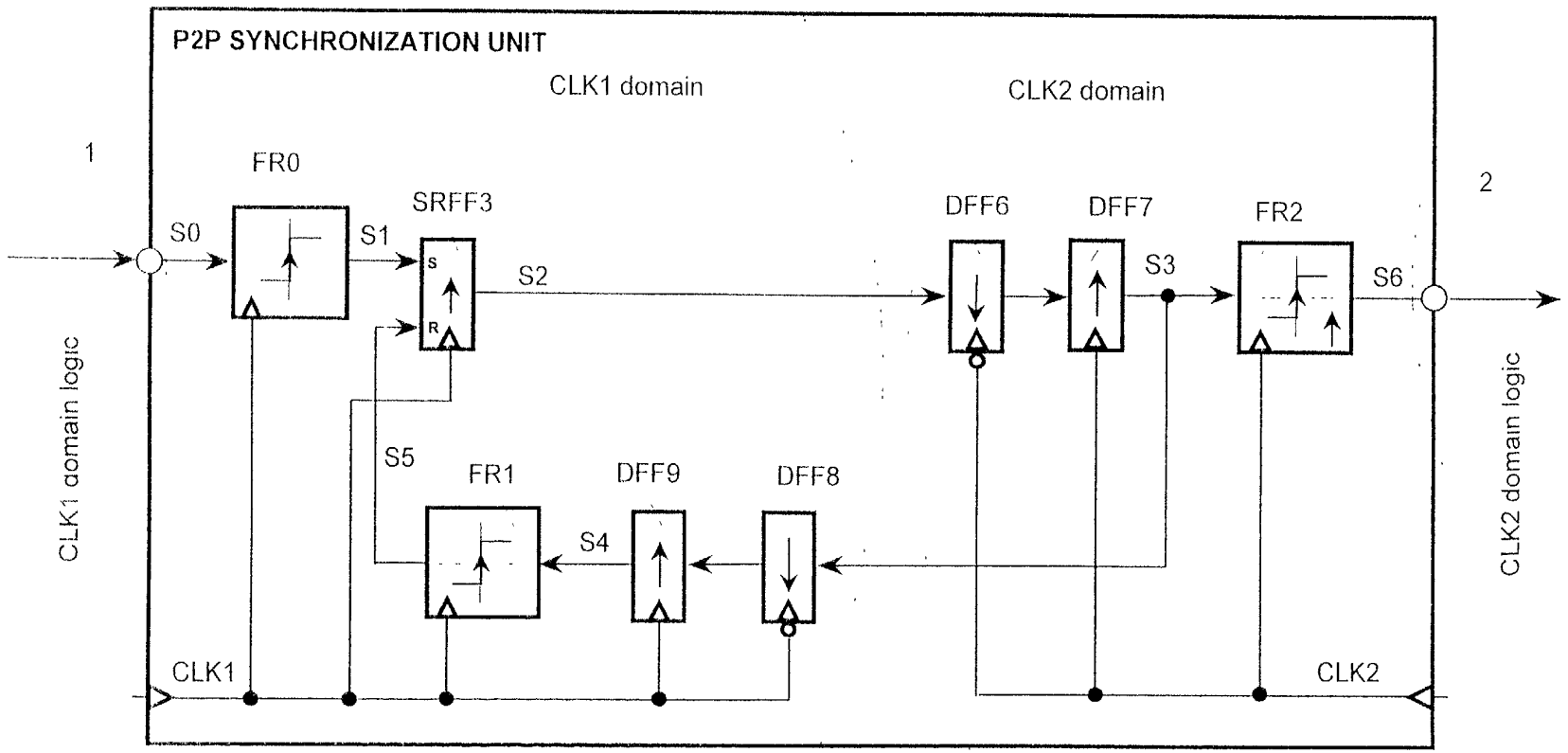


Figure 27

Timing Diagram of Pulse to Pulse Synchronization Unit

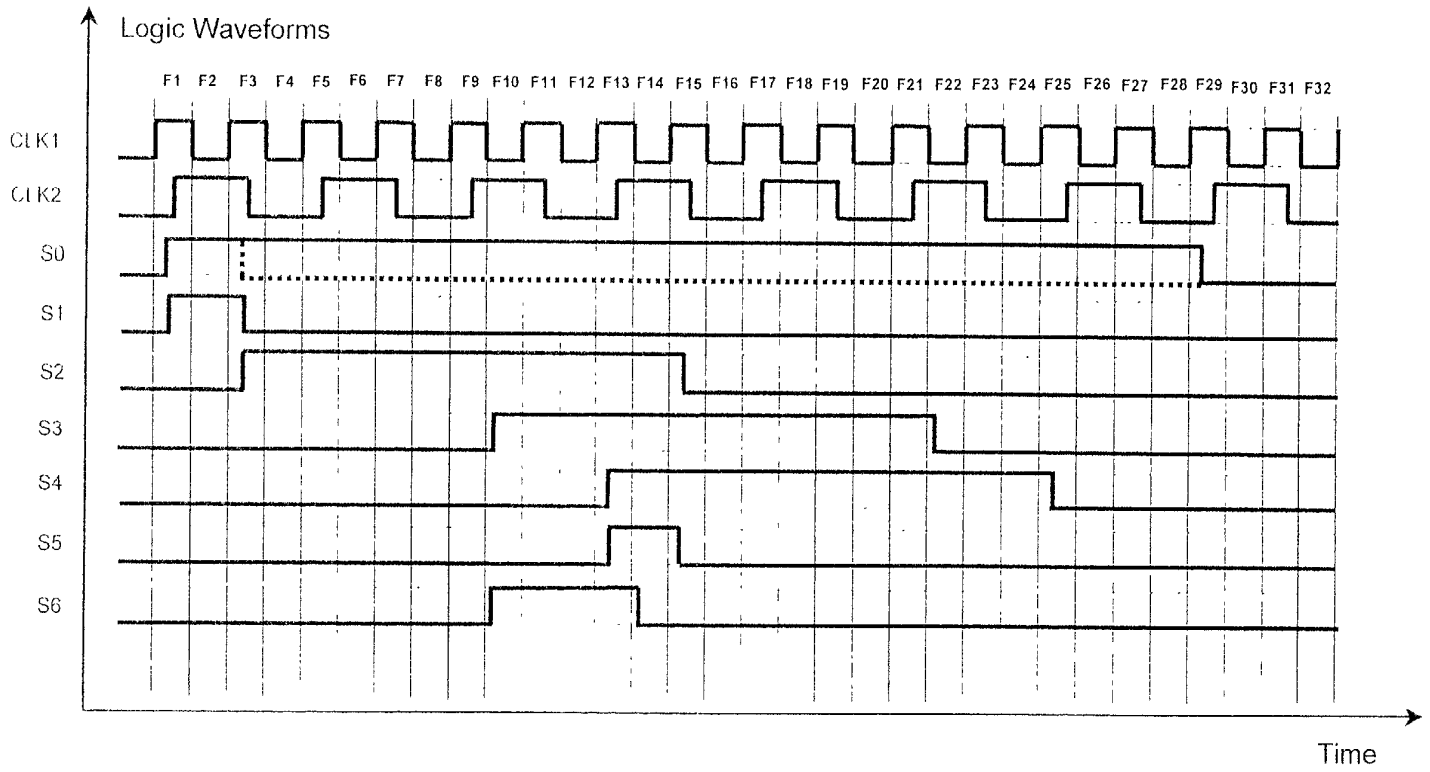


Figure 28

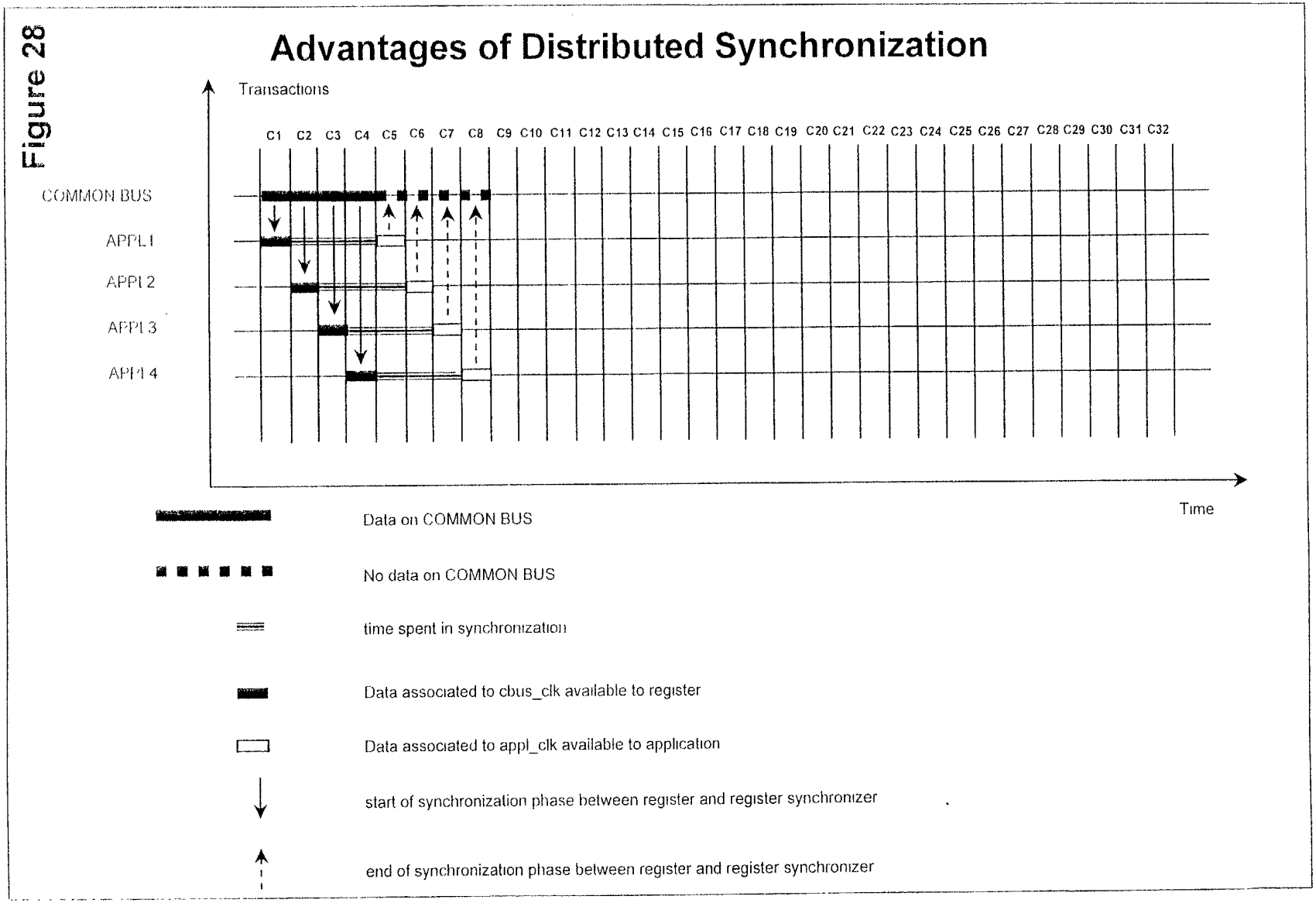

Advantages of Distributed Synchronization
Transactions
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32
COMMON BUS
APPL1
APPL2
APPL3
APPL4
Time
Data on COMMON BUS
No data on COMMON BUS
time spent in synchronization
Data associated to cbus_clk available to register
Data associated to appl_clk available to application
start of synchronization phase between register and register synchronizer
end of synchronization phase between register and register synchronizer

Figure29

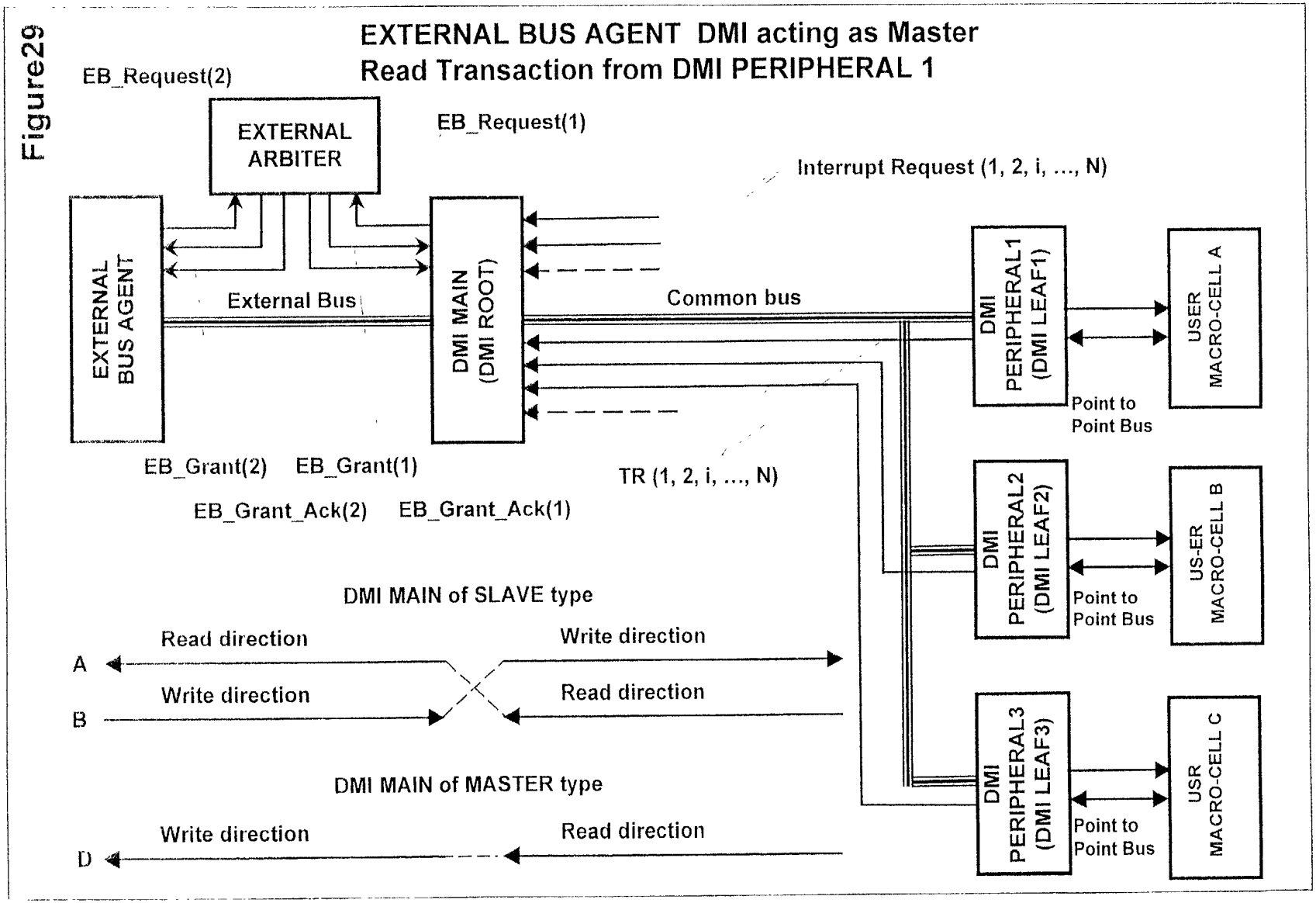
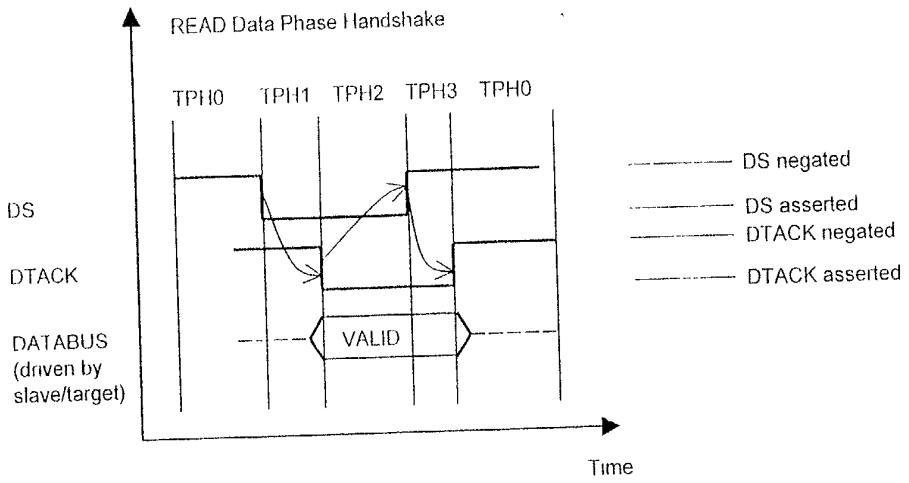

EXTERNAL BUS AGENT DMI acting as Master
Read Transaction from DMI PERIPHERAL 1
EB_Request(2)
EXTERNAL ARBITER
EB_Request(1)
Interrupt Request (1, 2, i, ..., N)
EXTERNAL BUS AGENT
External Bus
DMI MAIN (DMI ROOT)
Common bus
DMI PERIPHERAL1 (DMI LEAF1)
USER MACRO-CELL A
Point to Point Bus
EB_Grant(2)
EB_Grant(1)
TR (1, 2, i, ..., N)
EB_Grant_Ack(2)
EB_Grant_Ack(1)
DMI PERIPHERAL2 (DMI LEAF2)
US-ER MACRO-CELL B
Point to Point Bus
DMI MAIN of SLAVE type
Read direction
Write direction
A
Write direction
Read direction
B
DMI PERIPHERAL3 (DMI LEAF3)
USR MACRO-CELL C
Point to Point Bus
DMI MAIN of MASTER type
Write direction
Read direction
D

Figure 30

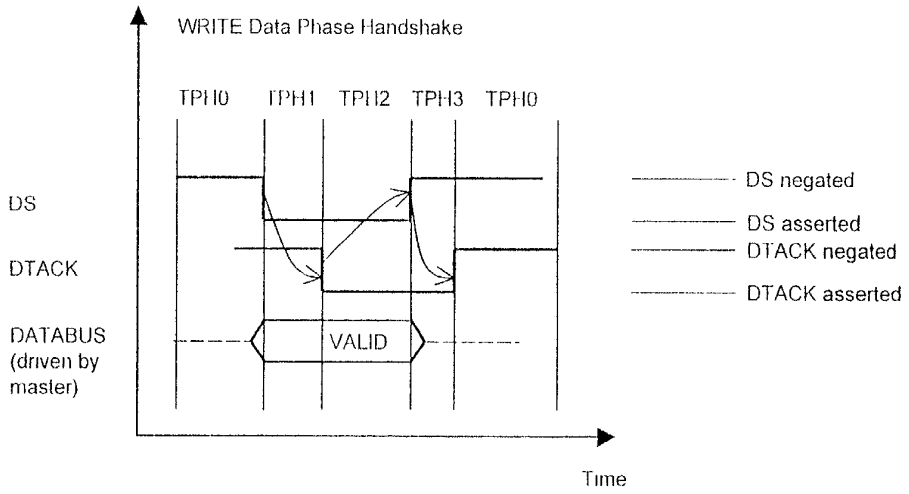
Asynchronous two phase handshake protocol: read



Prior Art

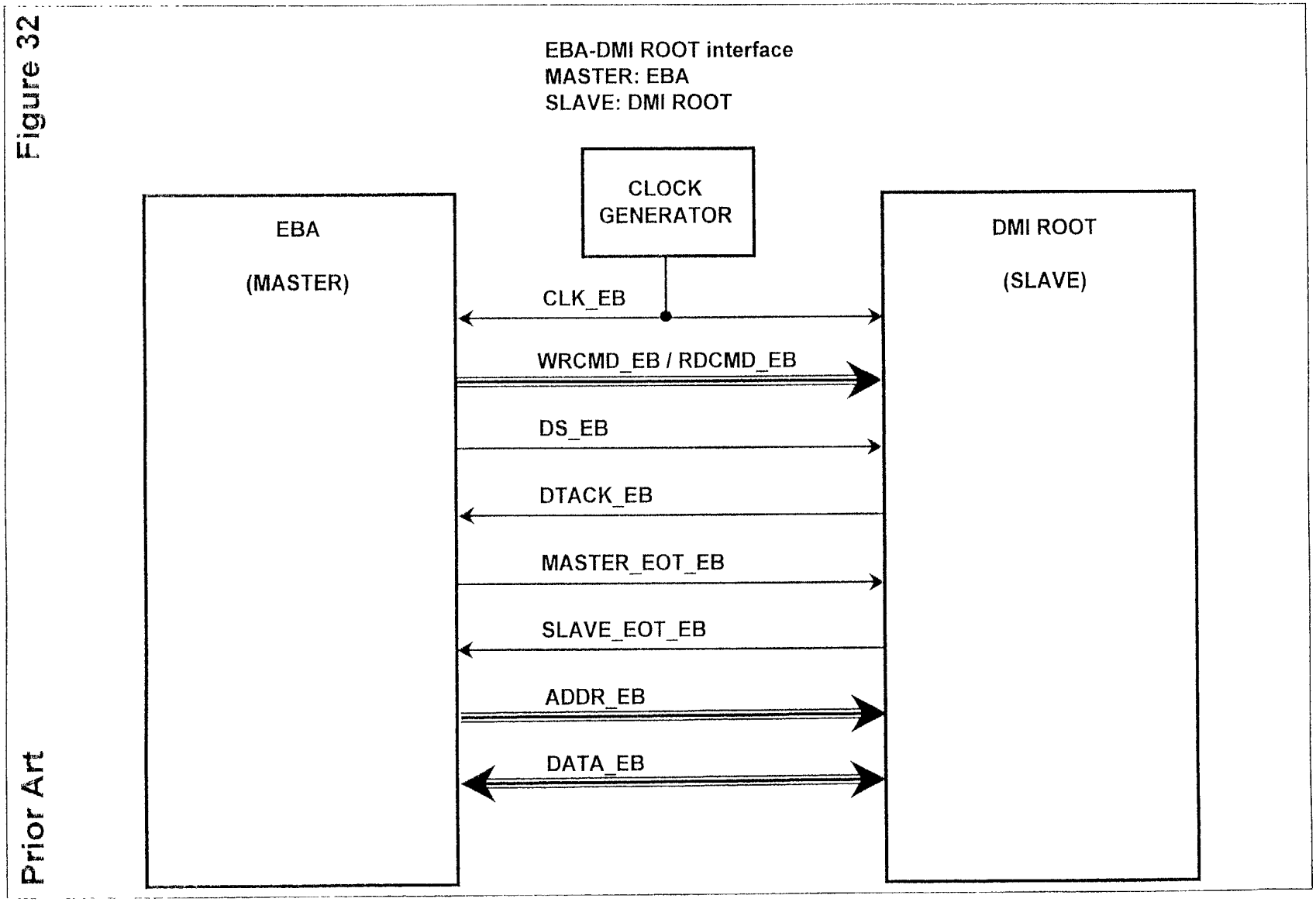
Figure 31

Asynchronous two phase handshake protocol: write



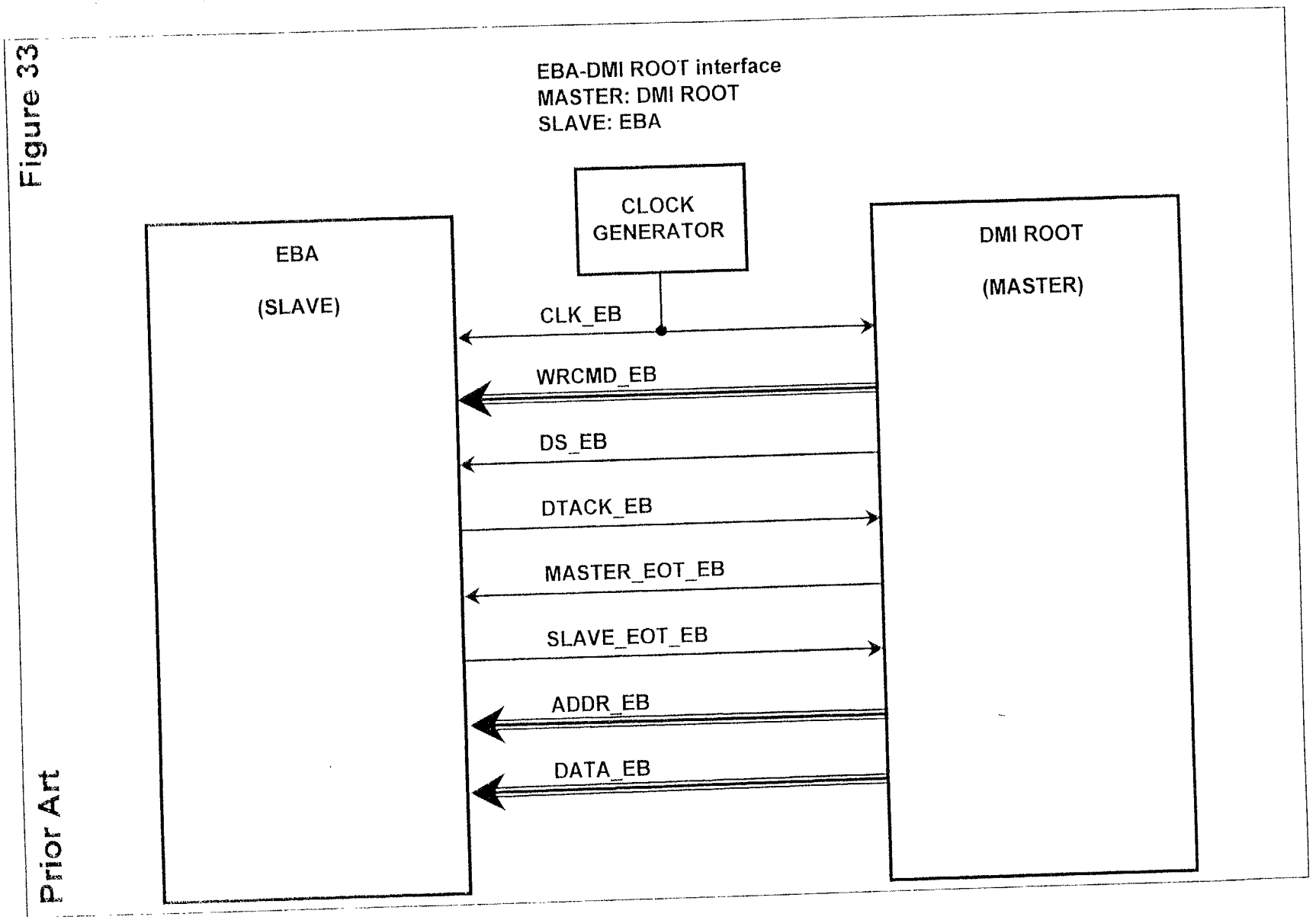
Prior Art

Figure 32



Prior Art

Figure 33



Prior Art

Figure 34

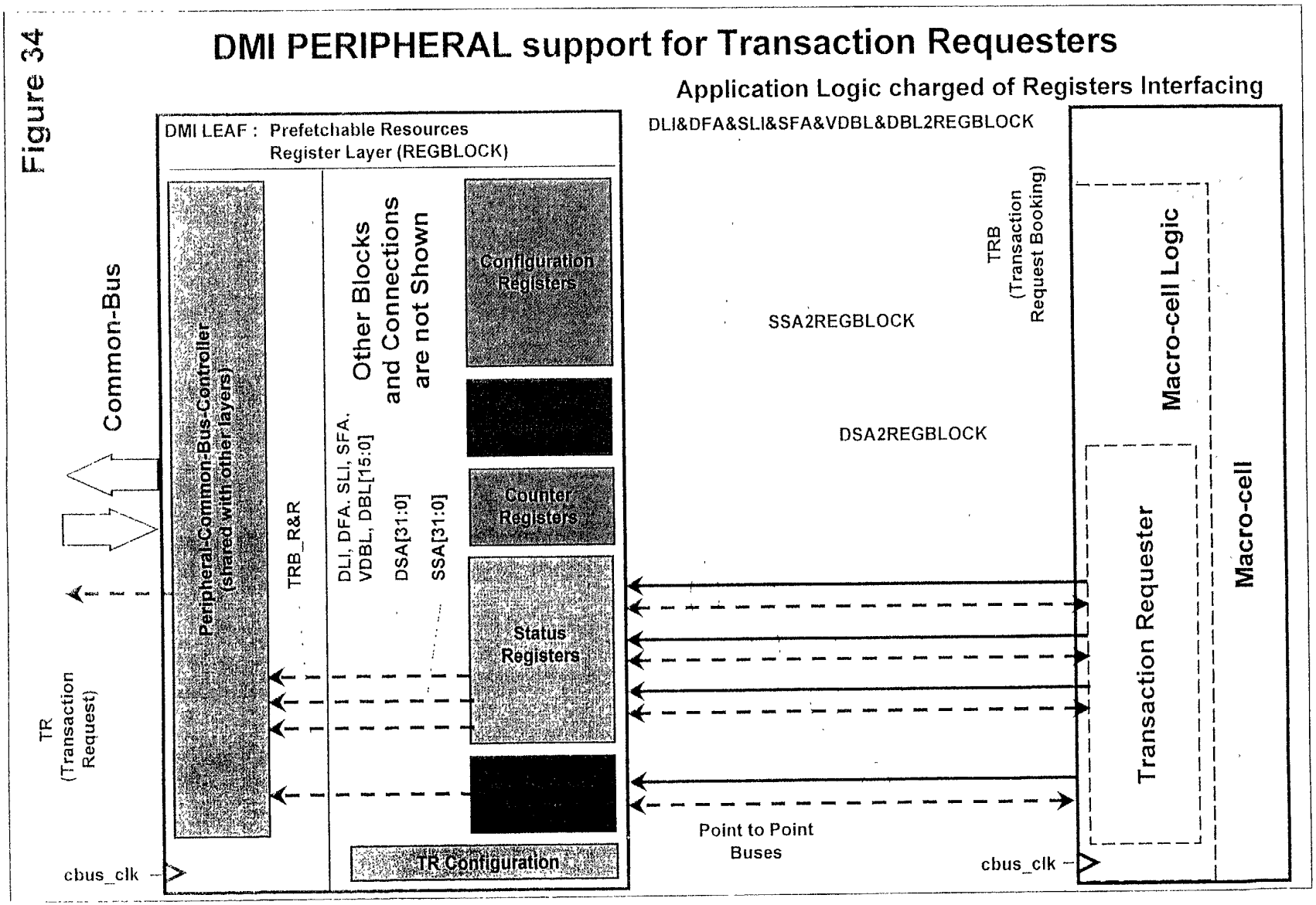
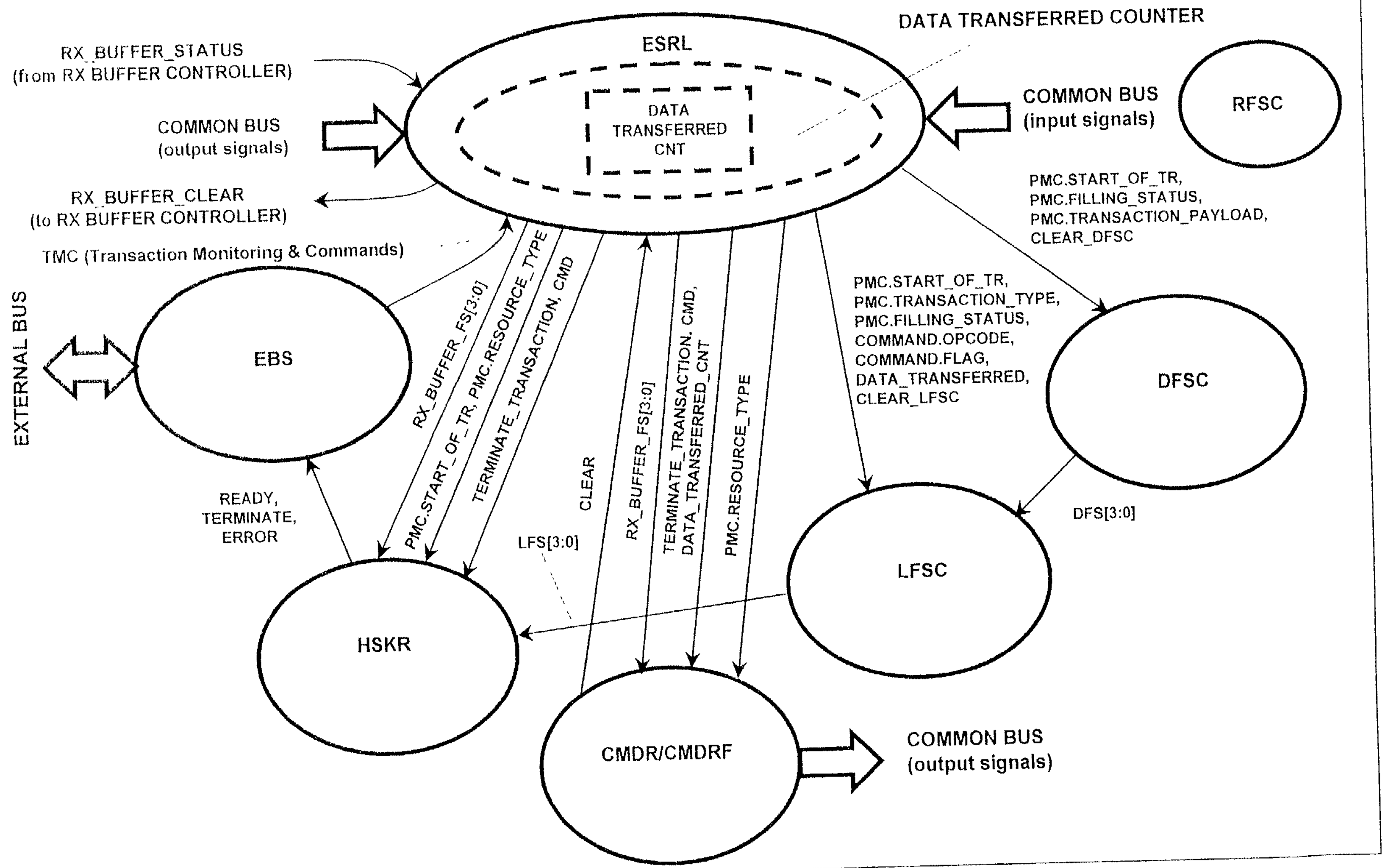

DMI PERIPHERAL support for Transaction Requesters
Application Logic charged of Registers Interfacing
DMI LEAF : Prefetchable Resources
Register Layer (REGBLOCK)
DLI&DFA&SLI&SFA&VDBL&DBL2REGBLOCK
Common-Bus
Peripheral Common Bus Controller (shared with other layers)
TRB_R&R
DLI, DFA, SLI, SFA, VDBL, DBL[15:0]
DSA[31:0]
SSA[31:0]
Other Blocks and Connections are not Shown
Configuration Registers
Counter Registers
Status Registers
TR Configuration
TR (Transaction Request)
cbus_clk
SSA2REGBLOCK
DSA2REGBLOCK
TRB (Transaction Request Booking)
Point to Point Buses
Macro-cell Logic
Transaction Requester
Macro-cell
cbus_clk

Figure 35

DMI Slave Mode Overall Algorithm Representation
Read Transaction from DMI PERIPHERAL + Read Transaction from EXTERNAL BUS AGENT


DATA TRANSFERRED COUNTER
ESRL
DATA TRANSFERRED CNT
RX_BUFFER_STATUS
(from RX BUFFER CONTROLLER)
COMMON BUS
(output signals)
RX_BUFFER_CLEAR
(to RX BUFFER CONTROLLER)
TMC (Transaction Monitoring & Commands)
COMMON BUS
(input signals)
RFSC
PMC.START_OF_TR,
PMC.FILLING_STATUS,
PMC.TRANSACTION_PAYLOAD,
CLEAR_DFSC
DFSC
PMC.START_OF_TR,
PMC.TRANSACTION_TYPE,
PMC.FILLING_STATUS,
COMMAND.OPCODE,
COMMAND.FLAG,
DATA_TRANSFERRED,
CLEAR_LFSC
DFS[3:0]
LFSC
EXTERNAL BUS
EBS
RX_BUFFER_FS[3:0]
PMC.START_OF_TR, PMC.RESOURCE_TYPE
TERMINATE_TRANSACTION, CMD
CLEAR
RX_BUFFER_FS[3:0]
TERMINATE_TRANSACTION. CMD,
DATA_TRANSFERRED_CNT
PMC.RESOURCE_TYPE
READY,
TERMINATE,
ERROR
LFS[3:0]
HSKR
CMDR/CMDRF
COMMON BUS
(output signals)

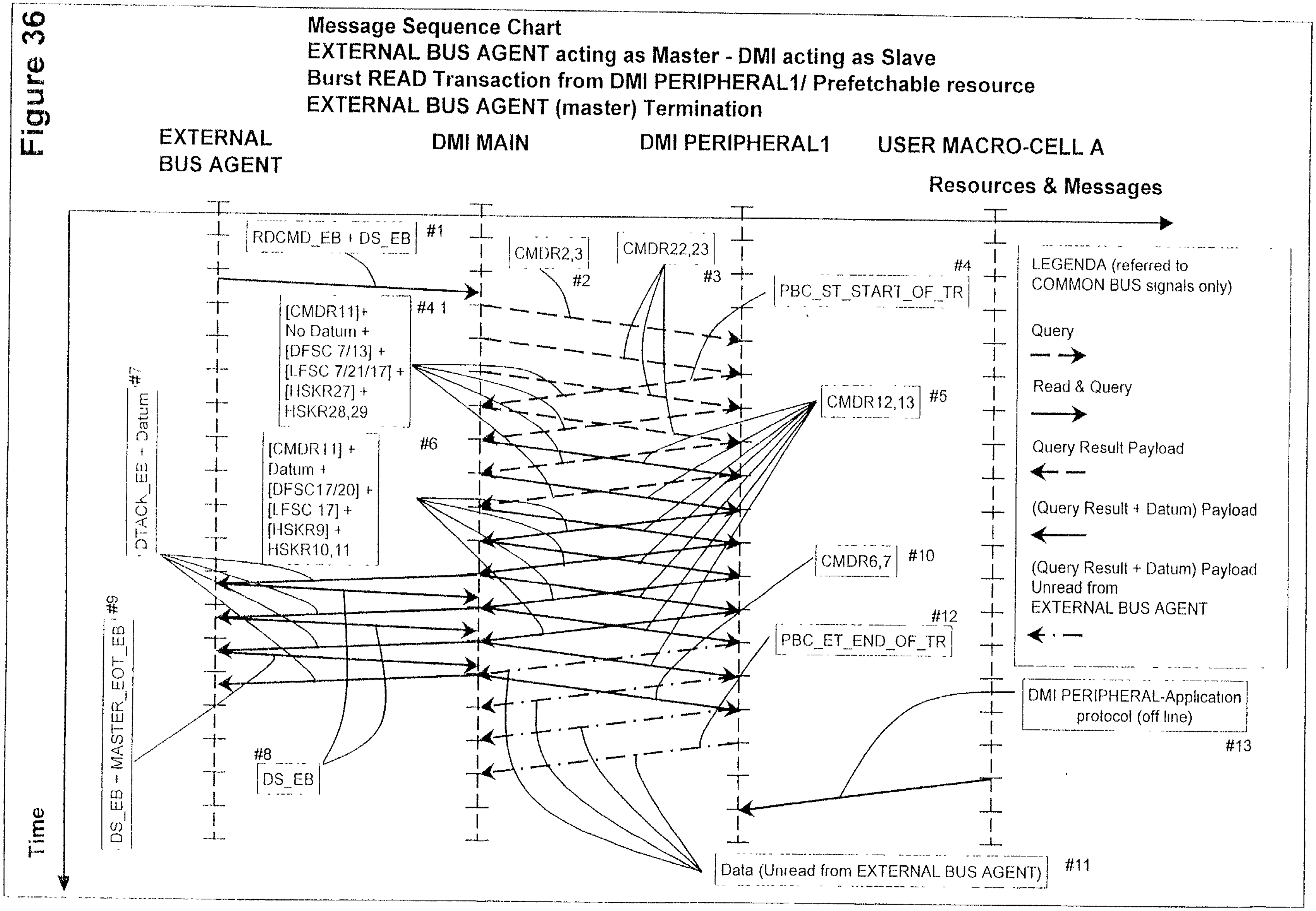

Message Sequence Chart
EXTERNAL BUS AGENT acting as Master - DMI acting as Slave
Burst READ Transaction from DMI PERIPHERAL1/ Prefetchable resource
EXTERNAL BUS AGENT (master) Termination
EXTERNAL BUS AGENT
DMI MAIN
DMI PERIPHERAL1
USER MACRO-CELL A
Resources & Messages
RDCMD_EB + DS_EB #1
CMDR2,3 #2
CMDR22,23 #3
#4 PBC_ST_START_OF_TR
#4 1
[CMDR11]+ No Datum + [DFSC 7/13] + [LFSC 7/21/17] + [HSKR27] + HSKR28,29
CMDR12,13 #5
#6
[CMDR11] + Datum + [DFSC17/20] + [LFSC 17] + [HSKR9] + HSKR10,11
DTACK_EB - Datum #7
#8 DS_EB
DS_EB - MASTER_EOT_EB #9
CMDR6,7 #10
#12 PBC_ET_END_OF_TR
Data (Unread from EXTERNAL BUS AGENT) #11
DMI PERIPHERAL-Application protocol (off line) #13
LEGENDA (referred to COMMON BUS signals only)
Query
Read & Query
Query Result Payload
(Query Result + Datum) Payload
(Query Result + Datum) Payload Unread from EXTERNAL BUS AGENT
Time

Figure 36

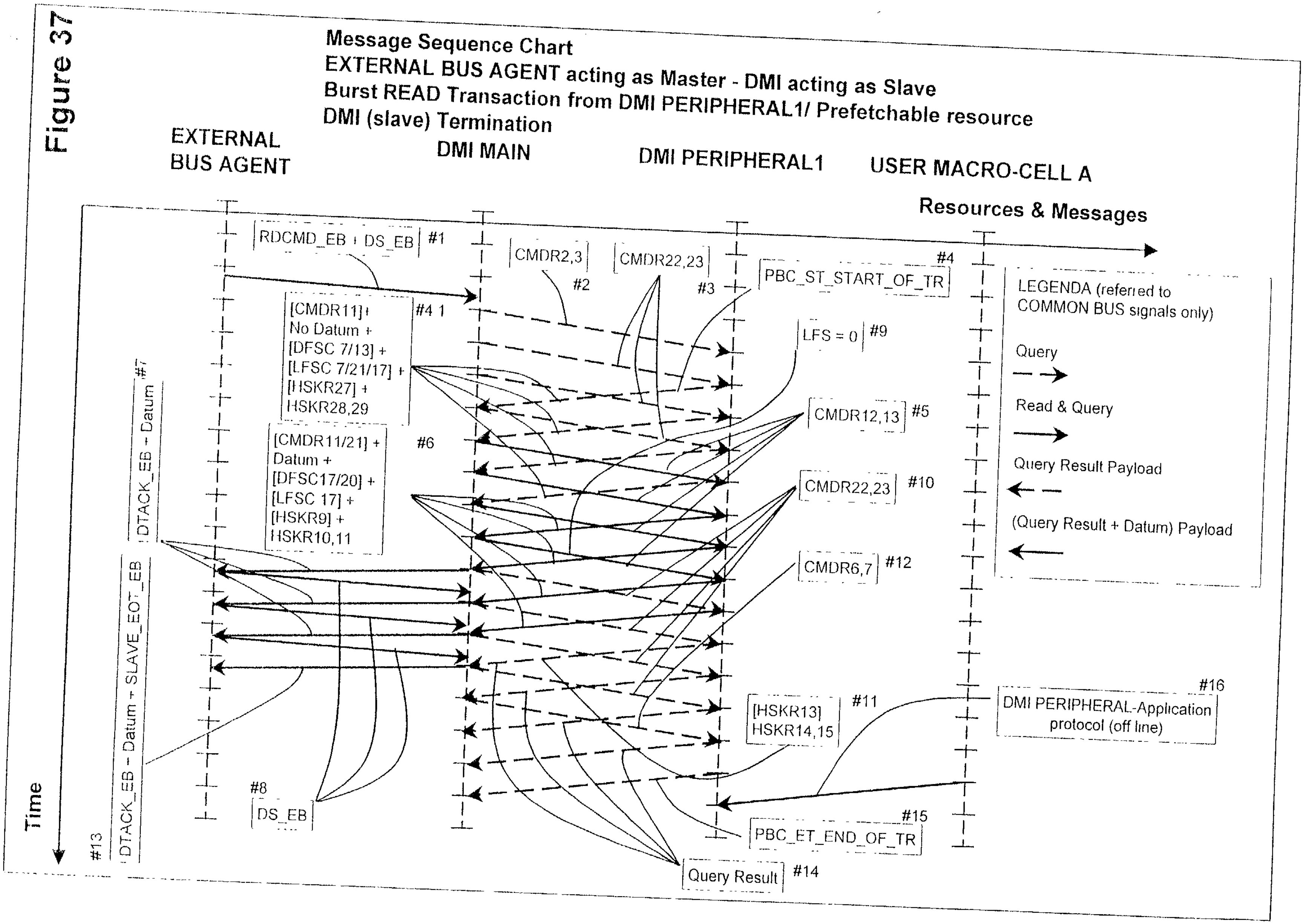

Message Sequence Chart
EXTERNAL BUS AGENT acting as Master - DMI acting as Slave
Burst READ Transaction from DMI PERIPHERAL1/ Prefetchable resource
DMI (slave) Termination
EXTERNAL BUS AGENT
DMI MAIN
DMI PERIPHERAL1
USER MACRO-CELL A
Resources & Messages
RDCMD_EB + DS_EB #1
CMDR2,3 #2
CMDR22,23 #3
PBC_ST_START_OF_TR #4
[CMDR11] + No Datum + [DFSC 7/13] + [LFSC 7/21/17] + [HSKR27] + HSKR28,29 #4 1
LFS = 0 #9
CMDR12,13 #5
[CMDR11/21] + Datum + [DFSC17/20] + [LFSC 17] + [HSKR9] + HSKR10,11 #6
CMDR22,23 #10
DTACK_EB - Datum #7
CMDR6,7 #12
DTACK_EB - Datum + SLAVE_EOT_EB #13
[HSKR13] HSKR14,15 #11
DMI PERIPHERAL-Application protocol (off line) #16
#8 DS_EB
PBC_ET_END_OF_TR #15
Query Result #14
LEGENDA (referred to COMMON BUS signals only)
Query
Read & Query
Query Result Payload
(Query Result + Datum) Payload
Time

Figure 37

Figure 38

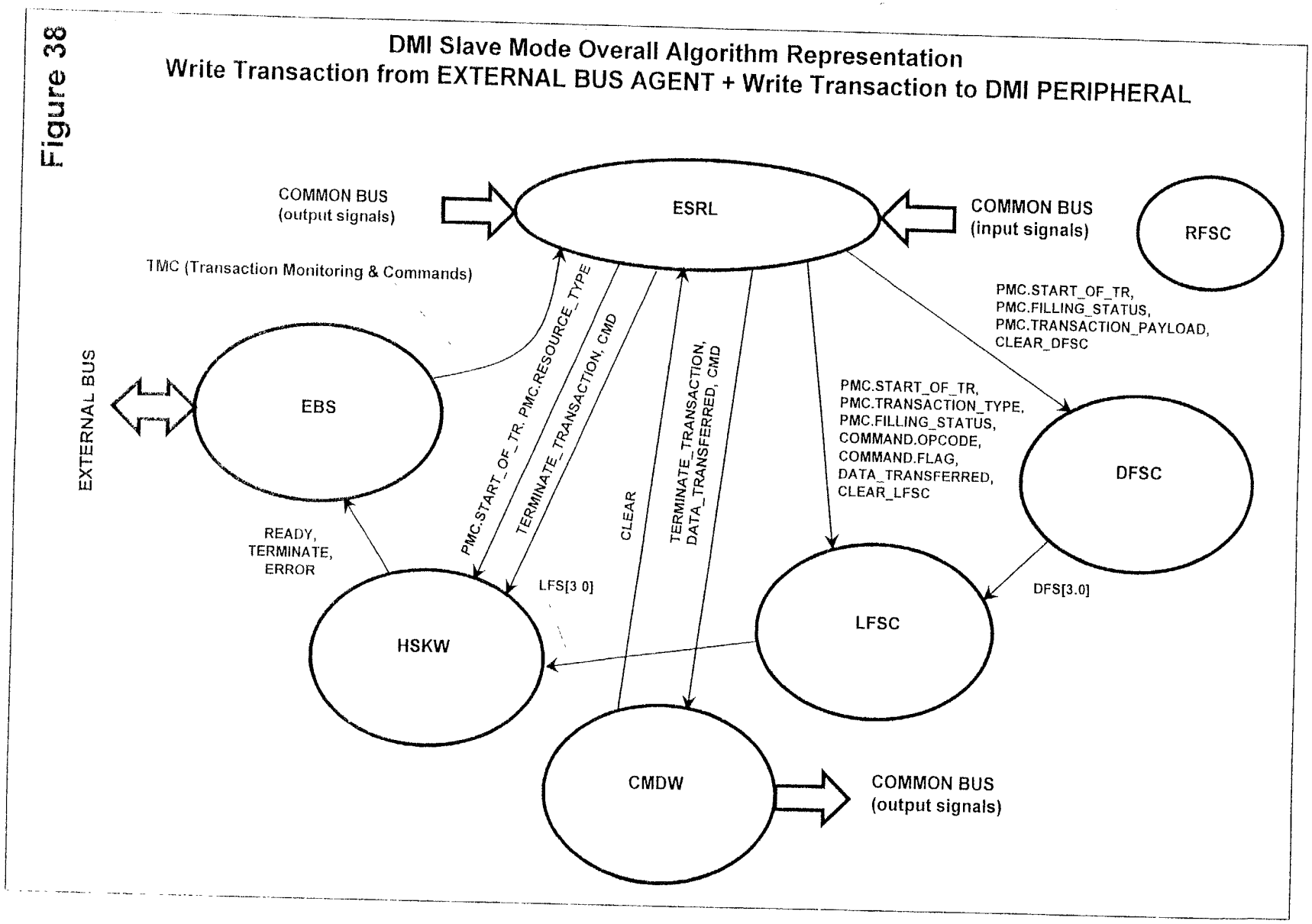

DMI Slave Mode Overall Algorithm Representation
Write Transaction from EXTERNAL BUS AGENT + Write Transaction to DMI PERIPHERAL
COMMON BUS
(output signals)
ESRL
COMMON BUS
(input signals)
RFSC
TMC (Transaction Monitoring & Commands)
PMC.START_OF_TR,
PMC.FILLING_STATUS,
PMC.TRANSACTION_PAYLOAD,
CLEAR_DFSC
EXTERNAL BUS
EBS
PMC.START_OF_TR, PMC.RESOURCE_TYPE
TERMINATE_TRANSACTION, CMD
CLEAR
TERMINATE_TRANSACTION,
DATA_TRANSFERRED, CMD
PMC.START_OF_TR,
PMC.TRANSACTION_TYPE,
PMC.FILLING_STATUS,
COMMAND.OPCODE,
COMMAND.FLAG,
DATA_TRANSFERRED,
CLEAR_LFSC
DFSC
READY,
TERMINATE,
ERROR
LFS[3 0]
DFS[3.0]
HSKW
LFSC
CMDW
COMMON BUS
(output signals)

Figure 39

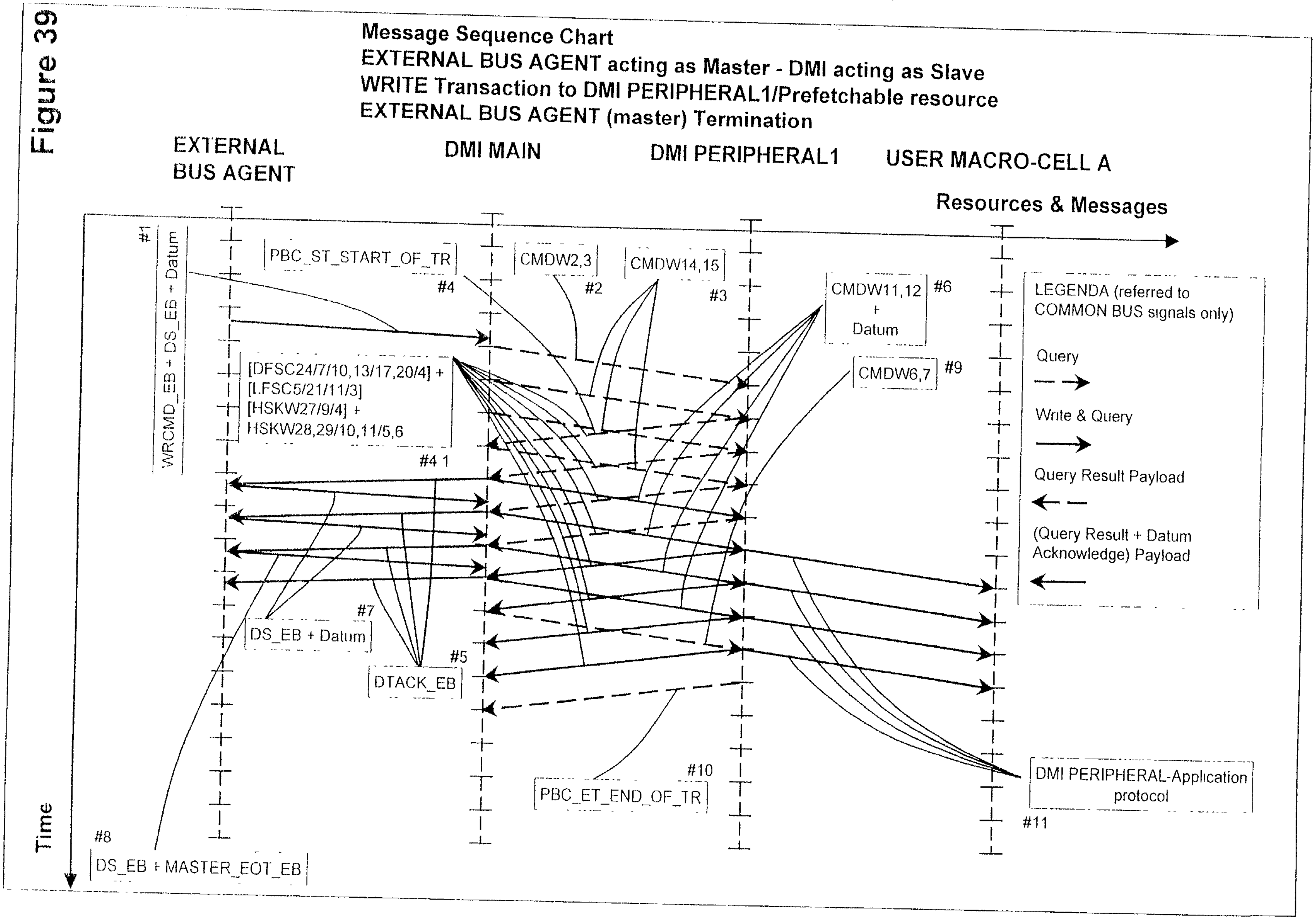

Message Sequence Chart
EXTERNAL BUS AGENT acting as Master - DMI acting as Slave
WRITE Transaction to DMI PERIPHERAL1/Prefetchable resource
EXTERNAL BUS AGENT (master) Termination
EXTERNAL BUS AGENT
DMI MAIN
DMI PERIPHERAL1
USER MACRO-CELL A
Resources & Messages
Time
#1
WRCMD_EB + DS_EB + Datum
PBC_ST_START_OF_TR
#4
CMDW2,3
#2
CMDW14,15
#3
CMDW11,12 + Datum
#6
CMDW6,7
#9
[DFSC24/7/10,13/17,20/4] +
[LFSC5/21/11/3]
[HSKW27/9/4] +
HSKW28,29/10,11/5,6
#4 1
DS_EB + Datum
#7
DTACK_EB
#5
PBC_ET_END_OF_TR
#10
#8
DS_EB + MASTER_EOT_EB
LEGENDA (referred to COMMON BUS signals only)
Query
Write & Query
Query Result Payload
(Query Result + Datum Acknowledge) Payload
DMI PERIPHERAL-Application protocol
#11

Figure 40

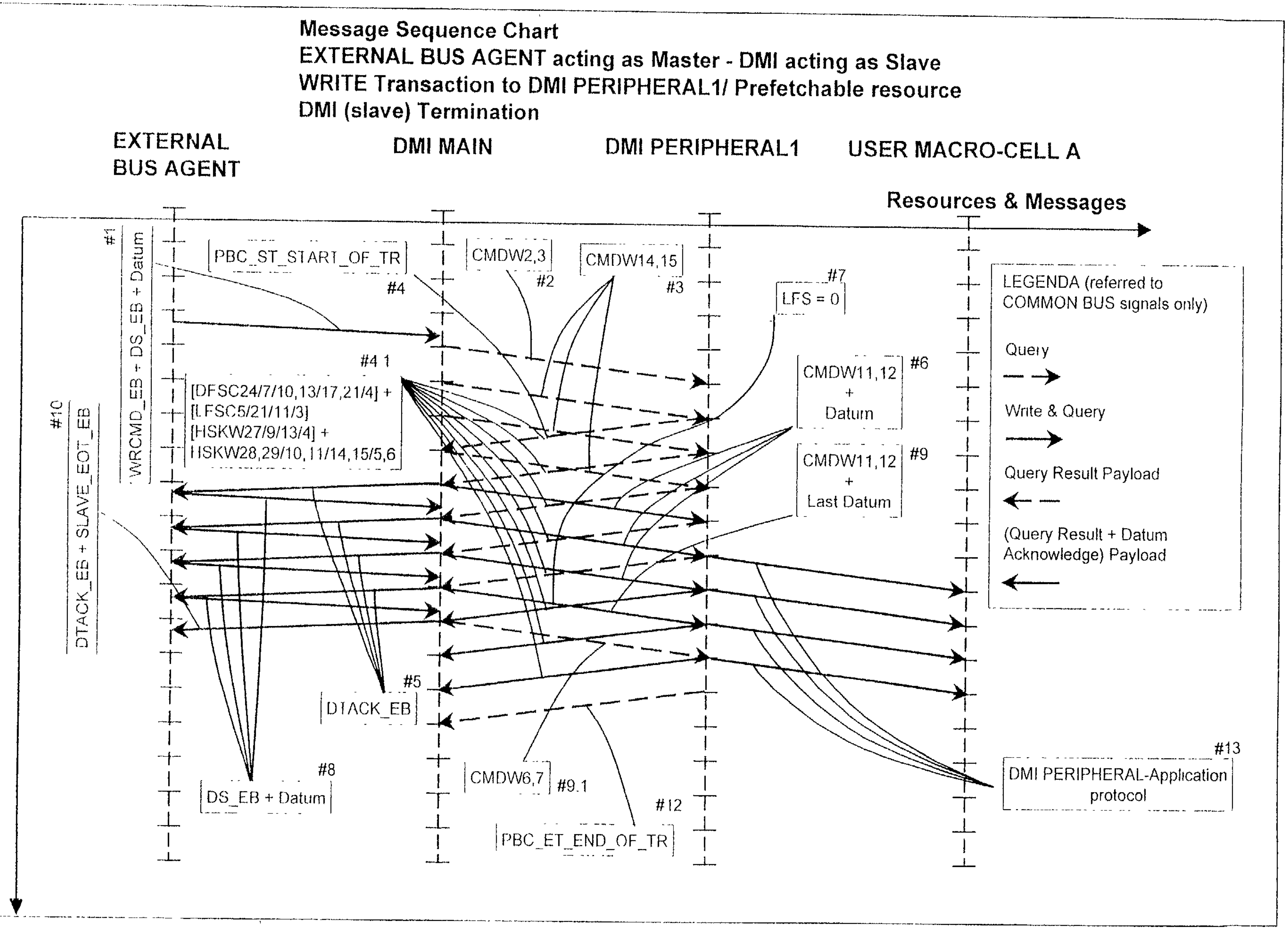

Message Sequence Chart
EXTERNAL BUS AGENT acting as Master - DMI acting as Slave
WRITE Transaction to DMI PERIPHERAL1/ Prefetchable resource
DMI (slave) Termination
EXTERNAL BUS AGENT
DMI MAIN
DMI PERIPHERAL1
USER MACRO-CELL A
Resources & Messages
Time
#1
WRCMD_EB + DS_EB + Datum
#10
DTACK_EB + SLAVE_EOT_EB
PBC_ST_START_OF_TR
#4
CMDW2,3
#2
CMDW14,15
#3
LFS = 0
#7
#4 1
[DFSC24/7/10,13/17,21/4] +
[LFSC5/21/11/3]
[HSKW27/9/13/4] +
HSKW28,29/10,11/14,15/5,6
CMDW11,12
+
Datum
#6
CMDW11,12
+
Last Datum
#9
#5
DTACK_EB
#8
DS_EB + Datum
CMDW6,7
#9.1
#12
PBC_ET_END_OF_TR
#13
DMI PERIPHERAL-Application protocol
LEGENDA (referred to COMMON BUS signals only)
Query
Write & Query
Query Result Payload
(Query Result + Datum Acknowledge) Payload

Figure 41

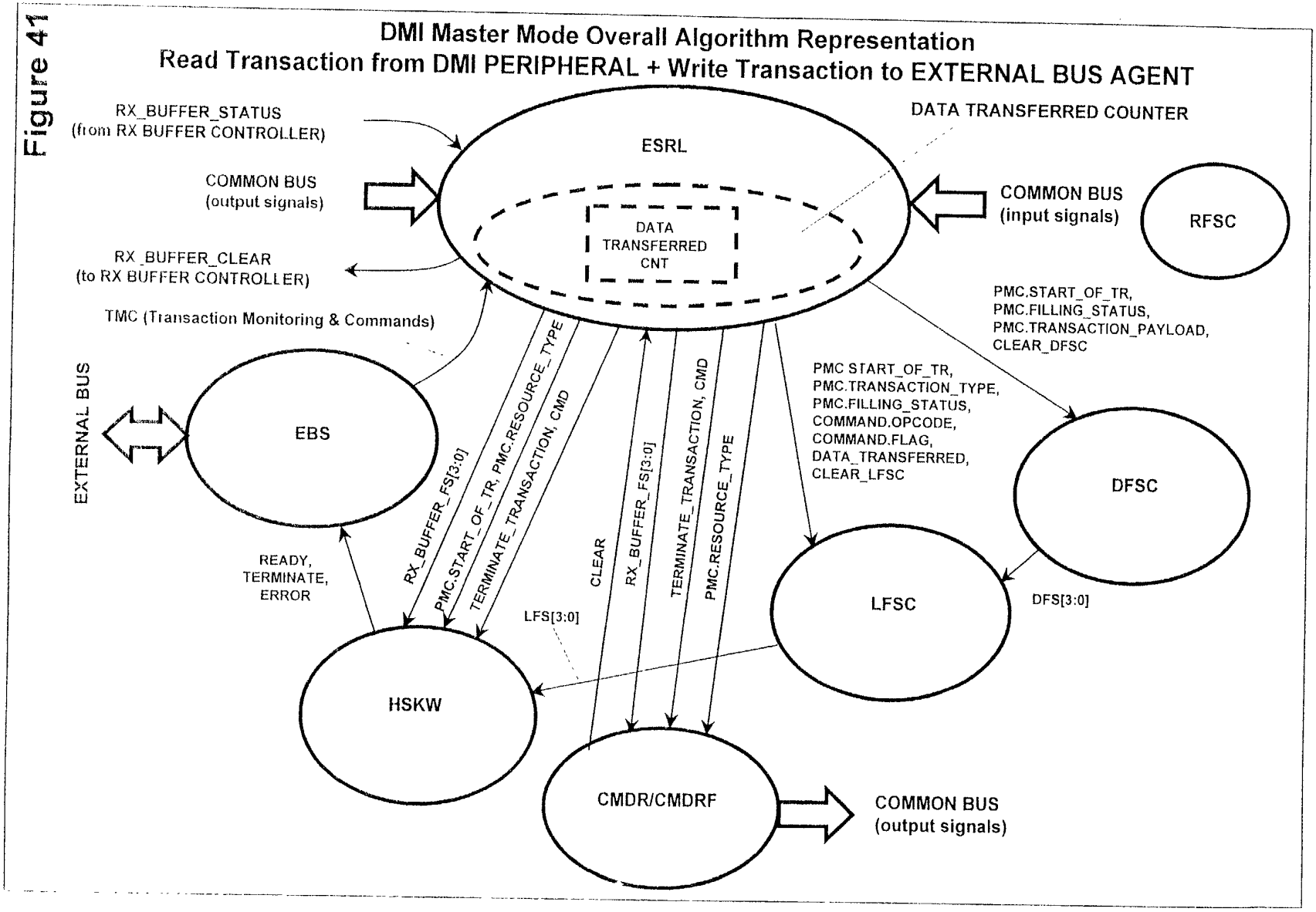

DMI Master Mode Overall Algorithm Representation
Read Transaction from DMI PERIPHERAL + Write Transaction to EXTERNAL BUS AGENT
RX_BUFFER_STATUS
(from RX BUFFER CONTROLLER)
COMMON BUS
(output signals)
RX_BUFFER_CLEAR
(to RX BUFFER CONTROLLER)
TMC (Transaction Monitoring & Commands)
EXTERNAL BUS
ESRL
DATA TRANSFERRED COUNTER
DATA TRANSFERRED CNT
COMMON BUS
(input signals)
RFSC
PMC.START_OF_TR,
PMC.FILLING_STATUS,
PMC.TRANSACTION_PAYLOAD,
CLEAR_DFSC
EBS
PMC START_OF_TR,
PMC.TRANSACTION_TYPE,
PMC.FILLING_STATUS,
COMMAND.OPCODE,
COMMAND.FLAG,
DATA_TRANSFERRED,
CLEAR_LFSC
DFSC
RX_BUFFER_FS[3:0]
PMC.START_OF_TR, PMC.RESOURCE_TYPE
TERMINATE_TRANSACTION, CMD
CLEAR
RX_BUFFER_FS[3:0]
TERMINATE_TRANSACTION, CMD
PMC.RESOURCE_TYPE
READY,
TERMINATE,
ERROR
LFS[3:0]
LFSC
DFS[3:0]
HSKW
CMDR/CMDRF
COMMON BUS
(output signals)

Figure 42

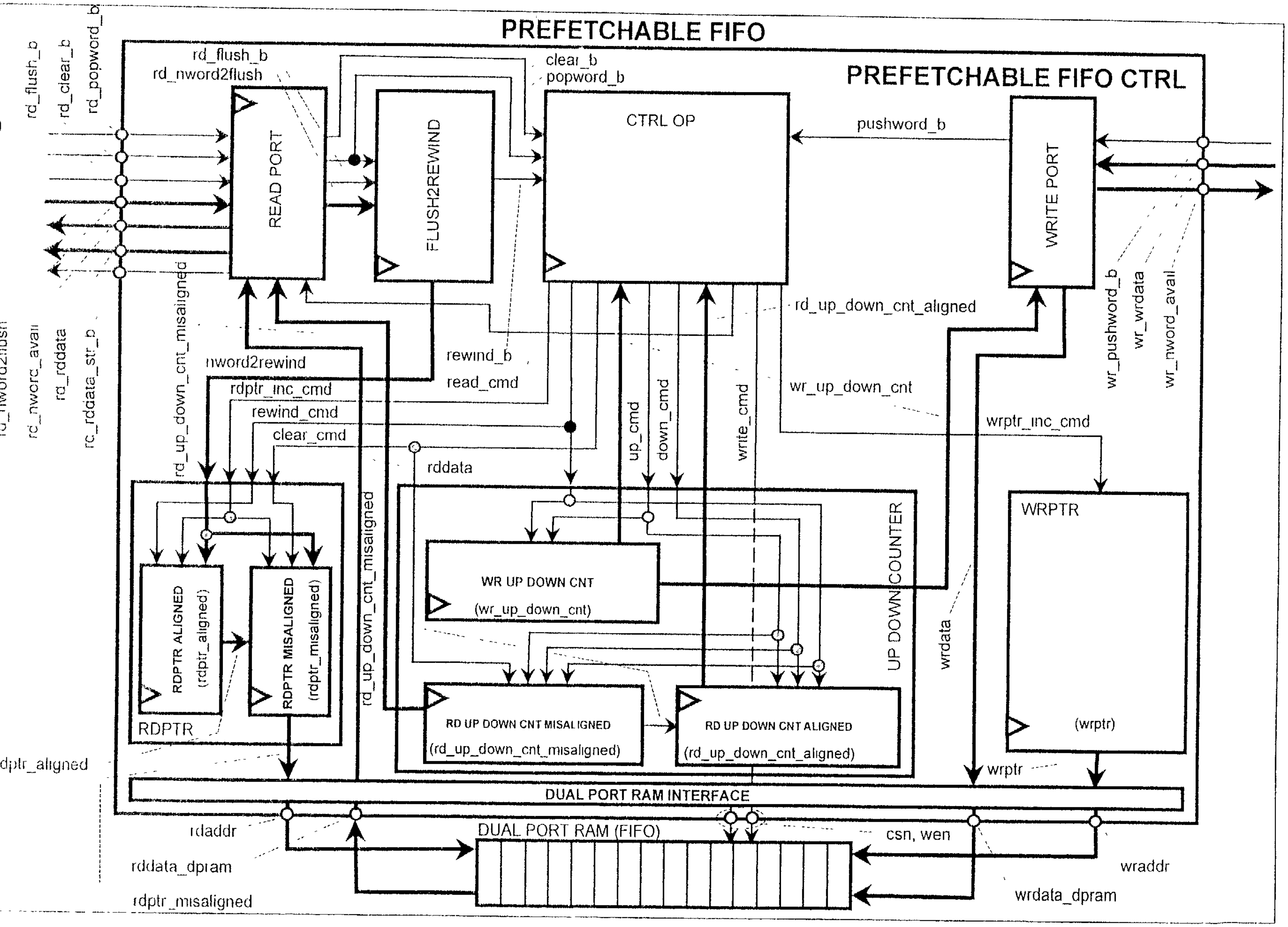

PREFETCHABLE FIFO
PREFETCHABLE FIFO CTRL
rd_flush_b
rd_clear_b
rd_popword_b
rd_nword2flush
rd_nworc_avail
rd_rddata
rc_rddata_str_b
rd_flush_b
rd_nword2flush
READ PORT
FLUSH2REWIND
clear_b
popword_b
CTRL OP
pushword_b
WRITE PORT
wr_pushword_b
wr_wrdata
wr_nword_avail
rd_up_down_cnt_aligned
wr_up_down_cnt
wrptr_inc_cmd
rd_up_down_cnt_misaligned
nword2rewind
rdptr_inc_cmd
rewind_cmd
clear_cmd
rewind_b
read_cmd
up_cmd
down_cmd
write_cmd
rddata
RDPTR ALIGNED
(rdptr_aligned)
RDPTR MISALIGNED
(rdptr_misaligned)
RDPTR
rd_up_down_cnt_misaligned
WR UP DOWN CNT
(wr_up_down_cnt)
RD UP DOWN CNT MISALIGNED
(rd_up_down_cnt_misaligned)
RD UP DOWN CNT ALIGNED
(rd_up_down_cnt_aligned)
UP DOWN COUNTER
wrdata
WRPTR
(wrptr)
wrptr
rdptr_aligned
DUAL PORT RAM INTERFACE
rdaddr
DUAL PORT RAM (FIFO)
csn, wen
rddata_dpram
wraddr
wrdata_dpram
rdptr_misaligned

Figure 43

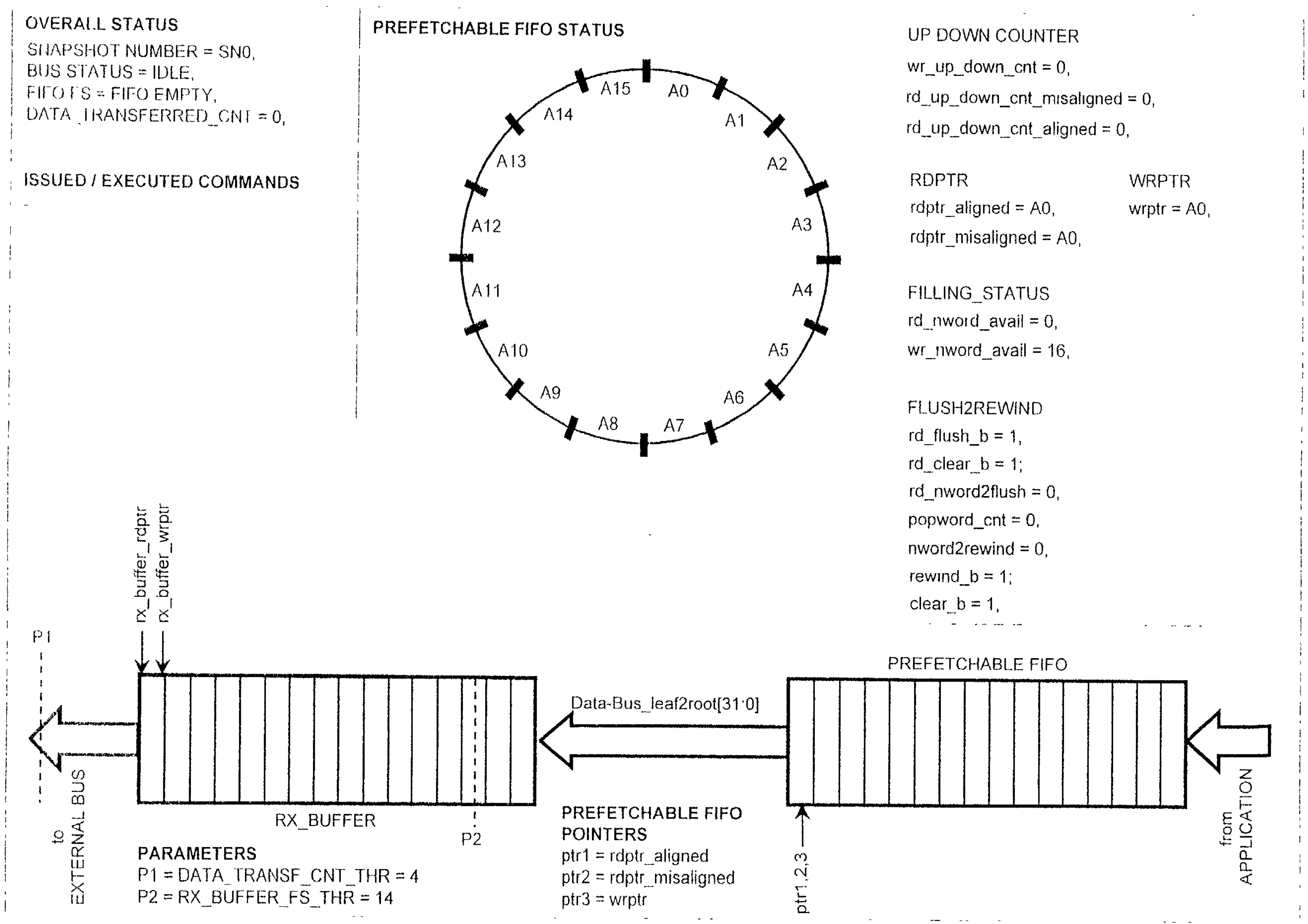

OVERALL STATUS
SNAPSHOT NUMBER = SN0,
BUS STATUS = IDLE,
FIFO FS = FIFO EMPTY,
DATA_TRANSFERRED_CNT = 0,
ISSUED / EXECUTED COMMANDS
PREFETCHABLE FIFO STATUS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
UP DOWN COUNTER
wr_up_down_cnt = 0,
rd_up_down_cnt_misaligned = 0,
rd_up_down_cnt_aligned = 0,
RDPTR
rdptr_aligned = A0,
rdptr_misaligned = A0,
WRPTR
wrptr = A0,
FILLING_STATUS
rd_nword_avail = 0,
wr_nword_avail = 16,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1;
rd_nword2flush = 0,
popword_cnt = 0,
nword2rewind = 0,
rewind_b = 1;
clear_b = 1,
rx_buffer_rdptr
rx_buffer_wrptr
P1
to EXTERNAL BUS
RX_BUFFER
P2
Data-Bus_leaf2root[31:0]
PREFETCHABLE FIFO
from APPLICATION
ptr1,2,3
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr

Figure 44

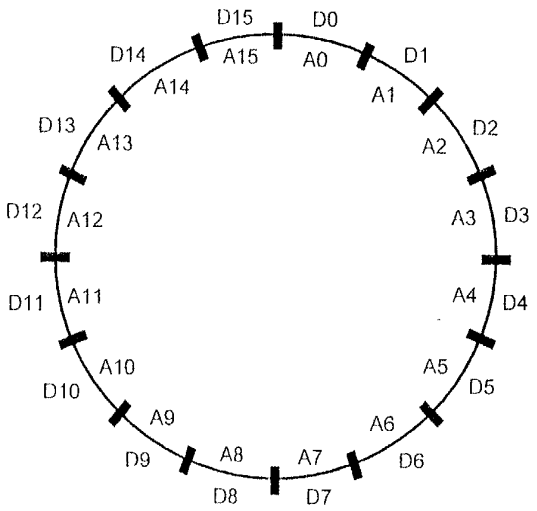
OVERALL STATUS

SNAPSHOT NUMBER = SN1,
BUS STATUS = WORKING,
FIFO FS = FIFO FULL,
DATA_TRANSFERRED_CNT = 0,

ISSUED / EXECUTED COMMANDS

16 FIFO PUSH EXECUTED,

PREFETCHABLE FIFO STATUS



UP DOWN COUNTER

wr_up_down_cnt = 16,
rd_up_down_cnt_misaligned = 16;
rd_up_down_cnt_aligned = 16,

RDPTR

rdptr_aligned = A0,
rdptr_misaligned = A0,

WRPTR

wrptr = A0
(one turn completed),

FILLING_STATUS

rd_nword_avail = 16;
wr_nword_avail = 0,

FLUSH2REWIND

rd_flush_b = 1,
rd_clear_b = 1,
rd_nword2flush = 0,
popword_cnt = 0;
nword2rewind = 0;
rewind_b = 1,
clear_b = 1,

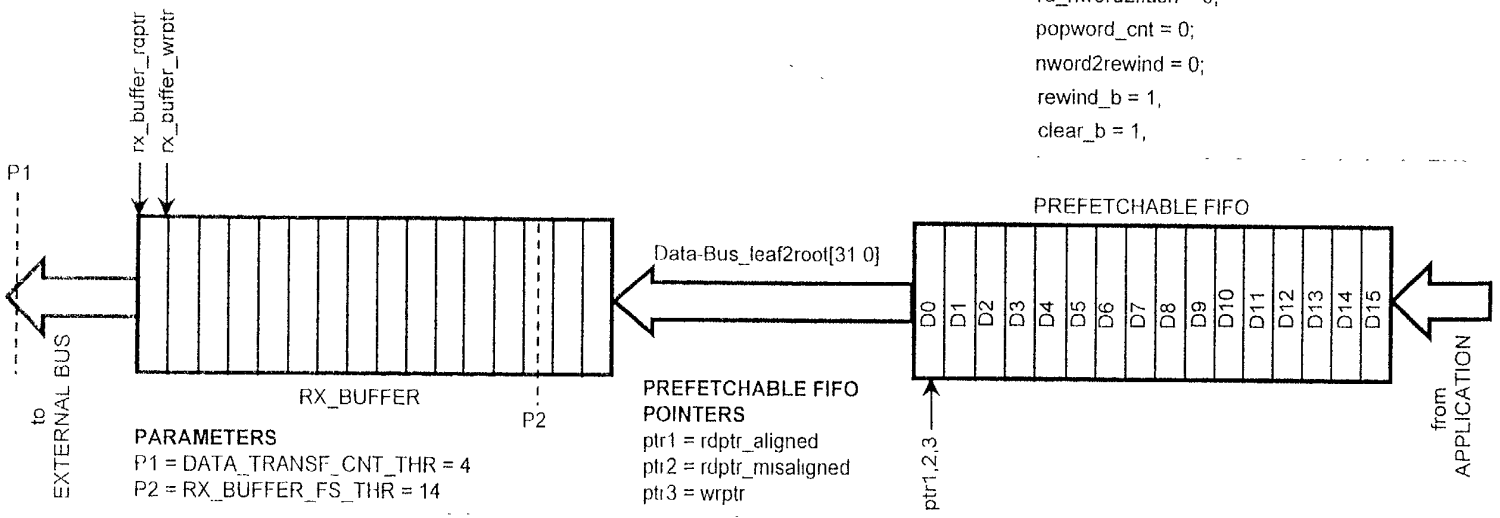


Figure 45

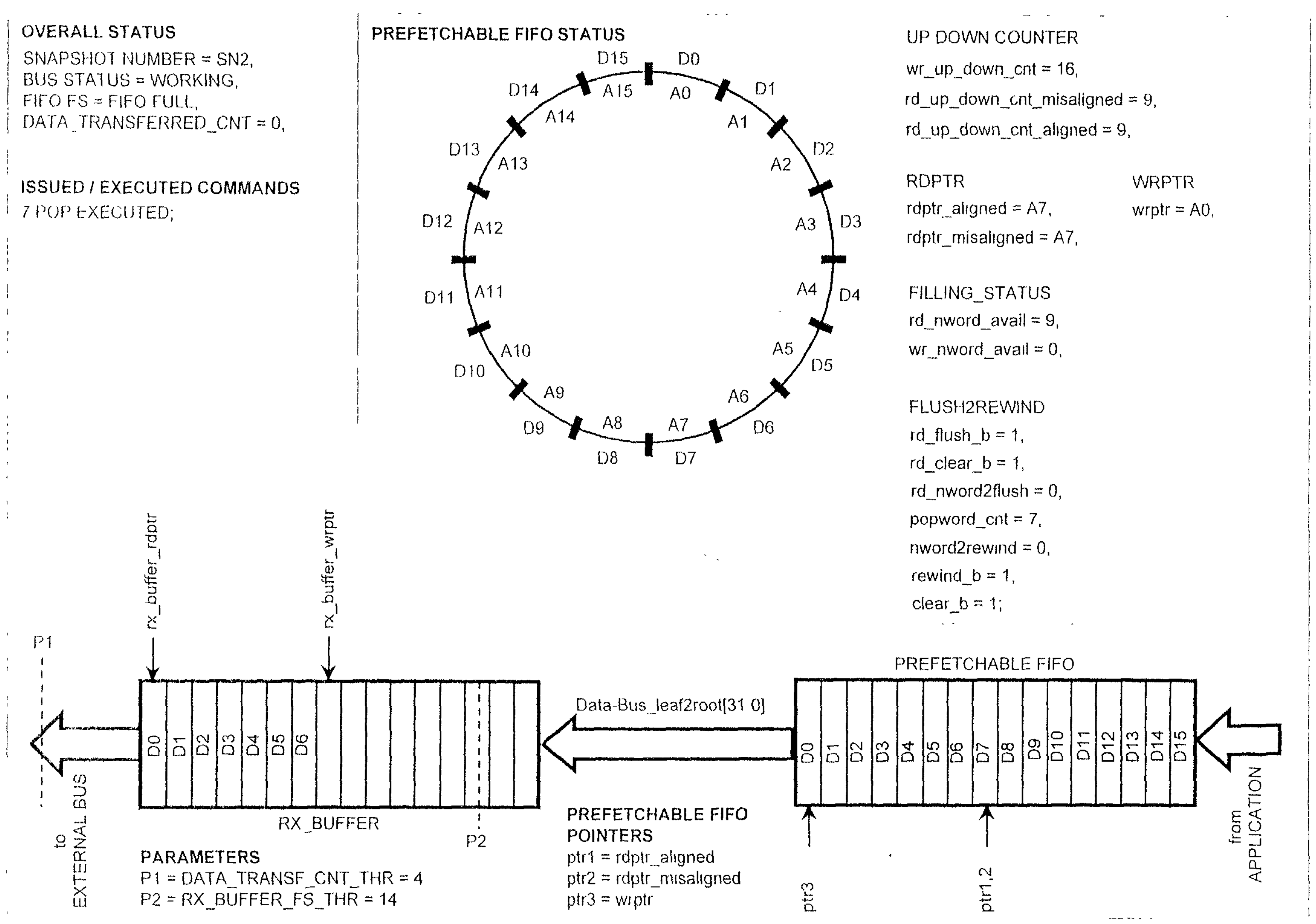
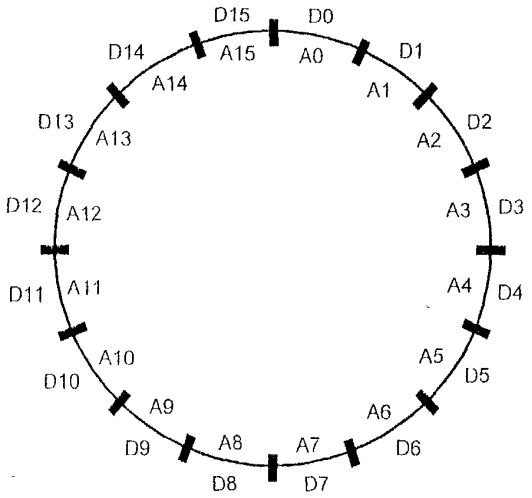

OVERALL STATUS
SNAPSHOT NUMBER = SN2,
BUS STATUS = WORKING,
FIFO FS = FIFO FULL,
DATA_TRANSFERRED_CNT = 0,
ISSUED / EXECUTED COMMANDS
7 POP EXECUTED;
PREFETCHABLE FIFO STATUS
D15 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
UP DOWN COUNTER
wr_up_down_cnt = 16,
rd_up_down_cnt_misaligned = 9,
rd_up_down_cnt_aligned = 9,
RDPTR
rdptr_aligned = A7,
rdptr_misaligned = A7,
WRPTR
wrptr = A0,
FILLING_STATUS
rd_nword_avail = 9,
wr_nword_avail = 0,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1,
rd_nword2flush = 0,
popword_cnt = 7,
nword2rewind = 0,
rewind_b = 1,
clear_b = 1;
P1
rx_buffer_rdptr
rx_buffer_wrptr
D0 D1 D2 D3 D4 D5 D6
RX_BUFFER
P2
to EXTERNAL BUS
Data-Bus_leaf2root[31 0]
PREFETCHABLE FIFO
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
from APPLICATION
ptr3
ptr1,2
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr

Figure 46

OVERALL STATUS
SNAPSHOT NUMBER = SN3,
BUS STATUS = WORKING,
FIFO FS = FIFO FULL,
DATA_TRANSFERRED_CNT = 4,

ISSUED / EXECUTED COMMANDS
FLUSH(4) ISSUED,

PREFETCHABLE FIFO STATUS



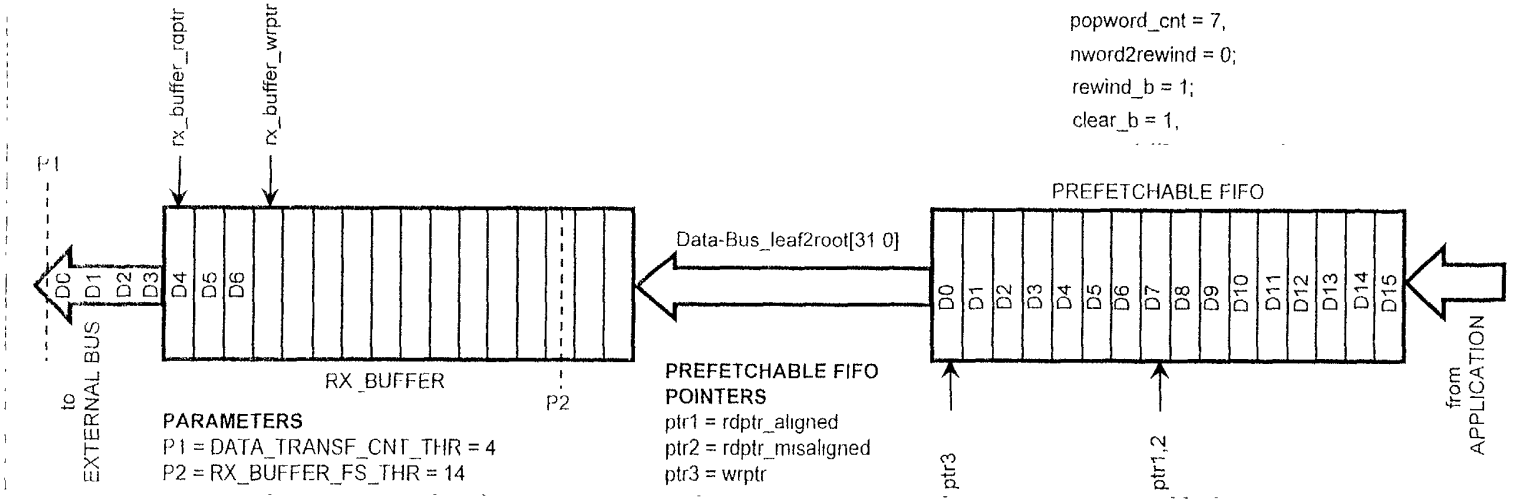
UP DOWN COUNTER
wr_up_down_cnt = 16,
rd_up_down_cnt_misaligned = 9,
rd_up_down_cnt_aligned = 9;

RDPTR
rdptr_aligned = A7,
rdptr_misaligned = A7;

WRPTR
wrptr = A0,

FILLING_STATUS
rd_nword_avail = 9,
wr_nword_avail = 0,

FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1;
rd_nword2flush = 0,
popword_cnt = 7,
nword2rewind = 0;
rewind_b = 1;
clear_b = 1,



PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14

PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr

Figure 47

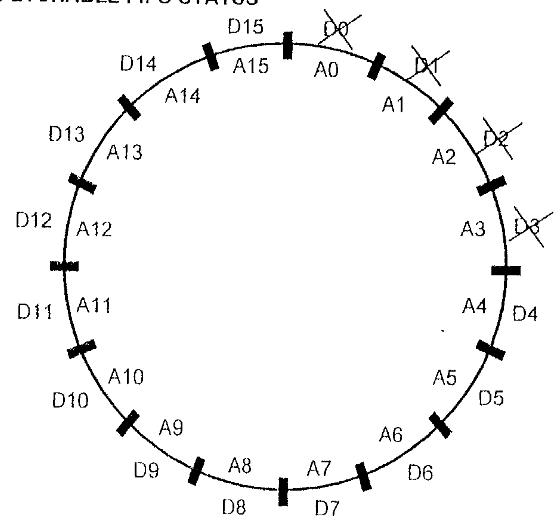
OVERALL STATUS

SNAPSHOT NUMBER = SN4,
BUS STATUS = WORKING,
FIFO FS = FIFO NOT FULL NOR EMPTY
DATA_TRANSFERRED_CNT = 0,

ISSUED / EXECUTED COMMANDS

FLUSH(4) EXECUTED
7 POP EXECUTED,
REWIND(3) EXECUTED,

PREFETCHABLE FIFO STATUS



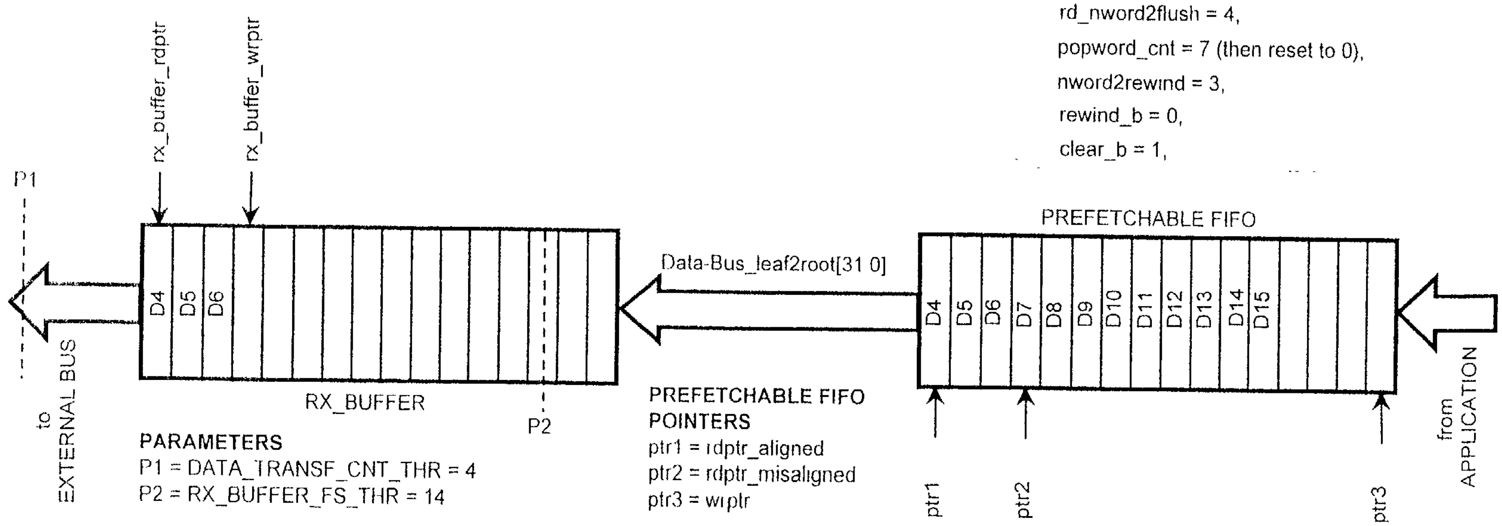
UP DOWN COUNTER
wr_up_down_cnt = 12,
rd_up_down_cnt_misaligned = 9,
rd_up_down_cnt_aligned = 12,

RDPTR
rdptr_aligned = A4,
rdptr_misaligned = A7,

WRPTR
wrptr = A0,

FILLING_STATUS
rd_nword_avail = 9,
wr_nword_avail = 4,

FLUSH2REWIND
rd_flush_b = 0,
rd_clear_b = 1,
rd_nword2flush = 4,
popword_cnt = 7 (then reset to 0),
nword2rewind = 3,
rewind_b = 0,
clear_b = 1,



PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14

PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr

Figure 48

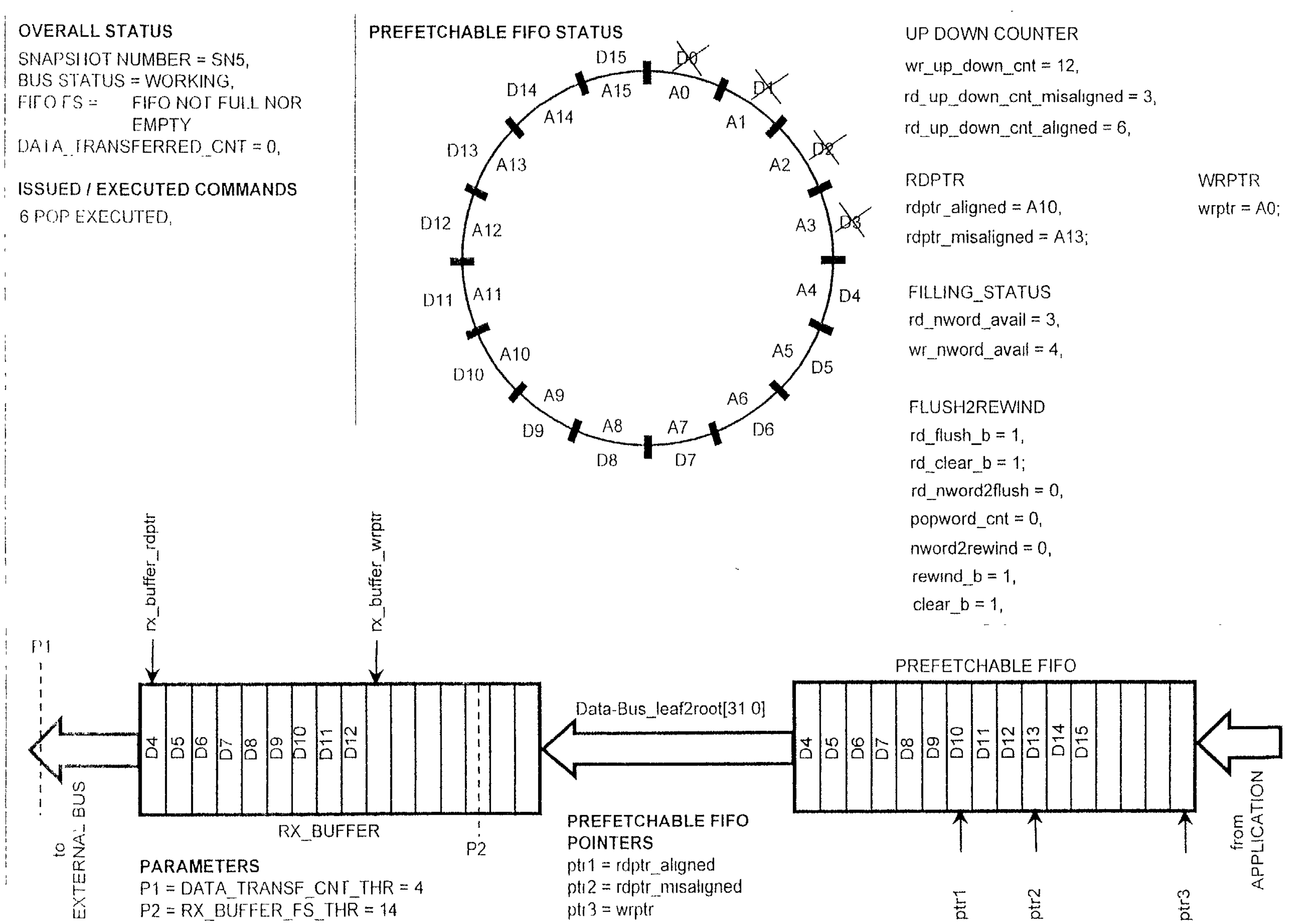
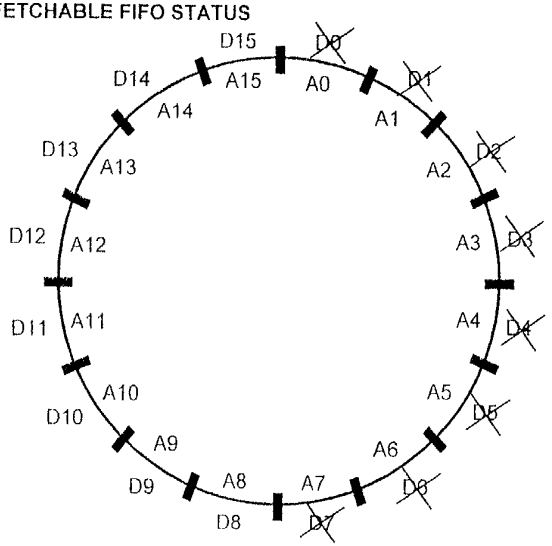

OVERALL STATUS
SNAPSHOT NUMBER = SN5,
BUS STATUS = WORKING,
FIFO FS = FIFO NOT FULL NOR EMPTY
DATA_TRANSFERRED_CNT = 0,
ISSUED / EXECUTED COMMANDS
6 POP EXECUTED,
PREFETCHABLE FIFO STATUS
D15 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
UP DOWN COUNTER
wr_up_down_cnt = 12,
rd_up_down_cnt_misaligned = 3,
rd_up_down_cnt_aligned = 6,
RDPTR
rdptr_aligned = A10,
rdptr_misaligned = A13;
WRPTR
wrptr = A0;
FILLING_STATUS
rd_nword_avail = 3,
wr_nword_avail = 4,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1;
rd_nword2flush = 0,
popword_cnt = 0,
nword2rewind = 0,
rewind_b = 1,
clear_b = 1,
P1
rx_buffer_rdptr
rx_buffer_wrptr
D4 D5 D6 D7 D8 D9 D10 D11 D12
to EXTERNAL BUS
RX_BUFFER
P2
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
Data-Bus_leaf2root[31 0]
PREFETCHABLE FIFO
D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
from APPLICATION
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr
ptr1
ptr2
ptr3

Figure 49

OVERALL STATUS
SNAPSHOT NUMBER = SN6,
BUS STATUS = WORKING,
FIFO FS = FIFO NOT FULL NOR EMPTY
DATA_TRANSFERRED_CNT = 4,

ISSUED / EXECUTED COMMANDS
CLEAR + FLUSH(4) EXECUTED
6 POP EXECUTED,
REWIND(2) EXECUTED;

PREFETCHABLE FIFO STATUS



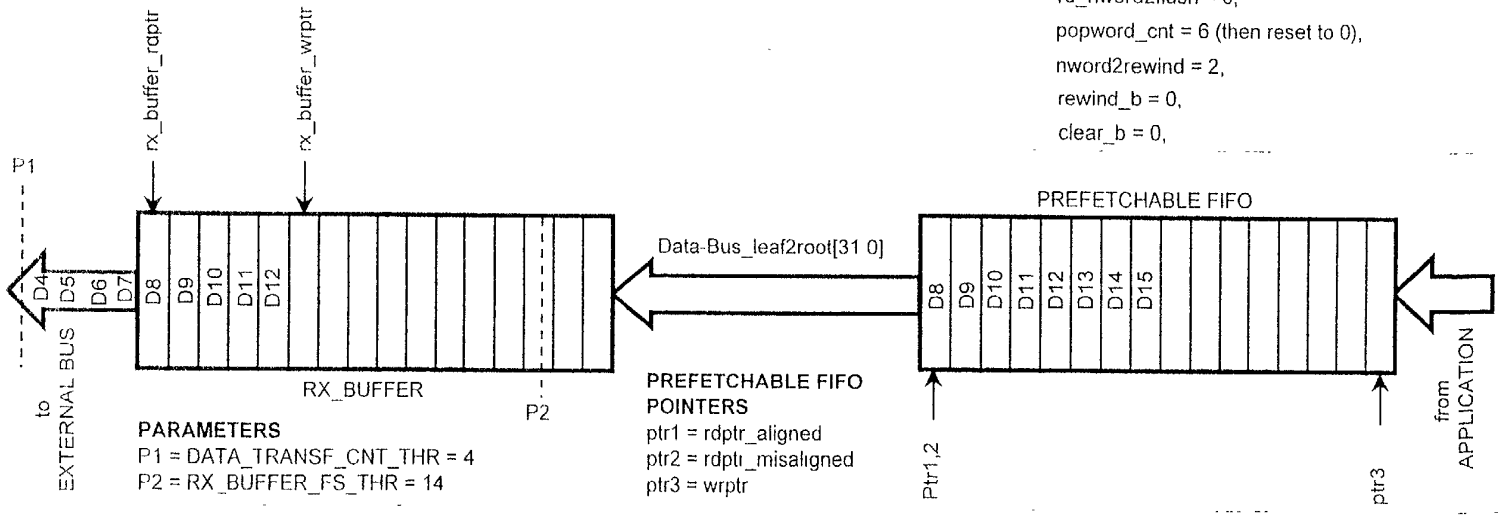
UP DOWN COUNTER
wr_up_down_cnt = 8,
rd_up_down_cnt_misaligned = 8,
rd_up_down_cnt_aligned = 8,

RDPTR
rdptr_aligned = A8,
rdptr_misaligned = A8;

WRPTR
wrptr = A0,

FILLING_STATUS
rd_nword_avail = 8,
wr_nword_avail = 8,

FLUSH2REWIND
rd_flush_b = 0,
rd_clear_b = 0,
rd_nword2flush = 0,
popword_cnt = 6 (then reset to 0),
nword2rewind = 2,
rewind_b = 0,
clear_b = 0,



PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14

PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr

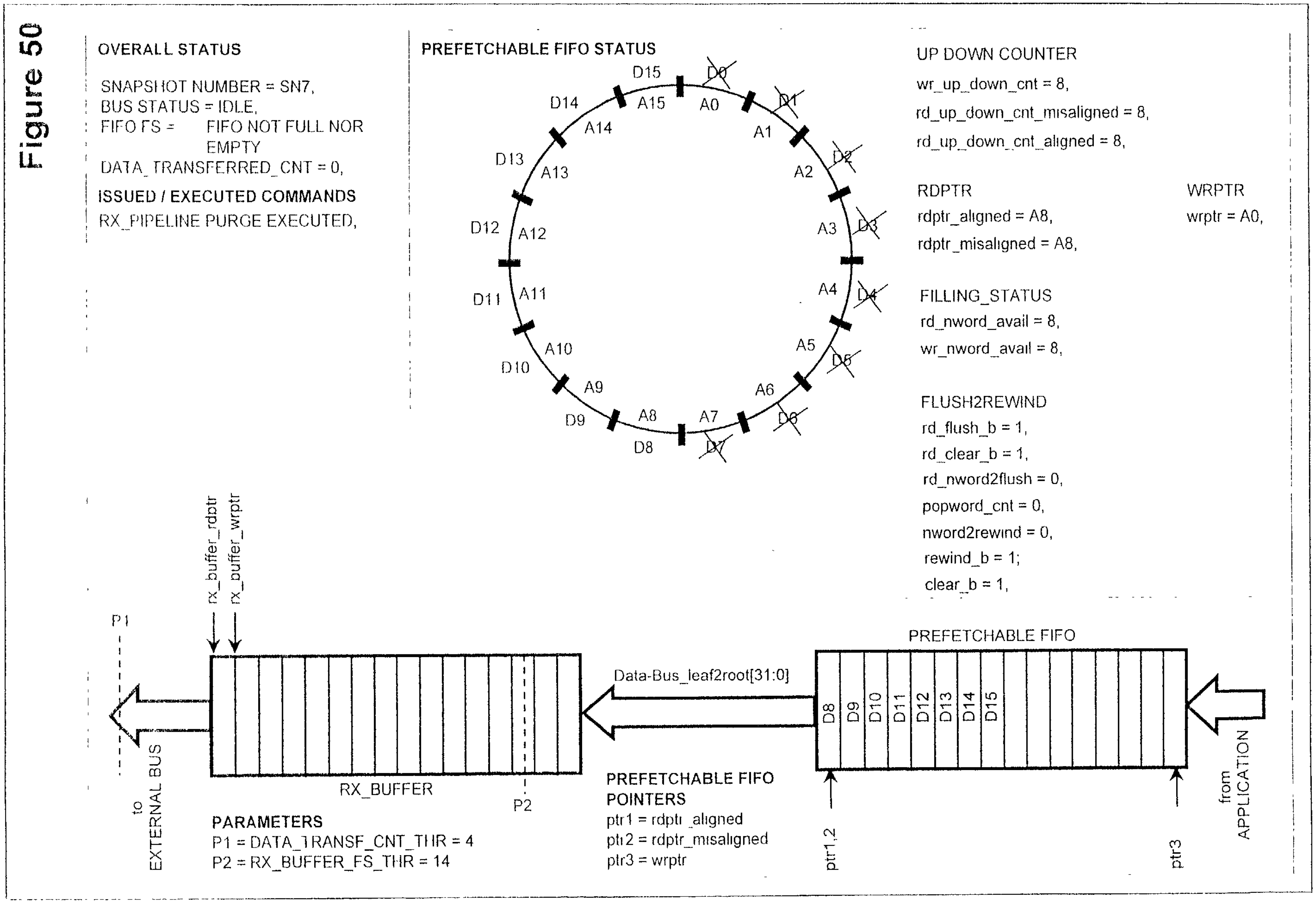

OVERALL STATUS
SNAPSHOT NUMBER = SN7,
BUS STATUS = IDLE,
FIFO FS = FIFO NOT FULL NOR EMPTY
DATA_TRANSFERRED_CNT = 0,
ISSUED / EXECUTED COMMANDS
RX_PIPELINE PURGE EXECUTED,
PREFETCHABLE FIFO STATUS
D15
D0
A15
A0
D14
D1
A14
A1
D13
D2
A13
A2
D12
A12
A3
D3
D11
A11
A4
D4
A10
A5
D10
D5
A9
A6
D9
A8
A7
D6
D8
D7
UP DOWN COUNTER
wr_up_down_cnt = 8,
rd_up_down_cnt_misaligned = 8,
rd_up_down_cnt_aligned = 8,
RDPTR
rdptr_aligned = A8,
rdptr_misaligned = A8,
WRPTR
wrptr = A0,
FILLING_STATUS
rd_nword_avail = 8,
wr_nword_avail = 8,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1,
rd_nword2flush = 0,
popword_cnt = 0,
nword2rewind = 0,
rewind_b = 1;
clear_b = 1,
rx_buffer_rdptr
rx_buffer_wrptr
P1
to EXTERNAL BUS
RX_BUFFER
P2
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
Data-Bus_leaf2root[31:0]
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr
PREFETCHABLE FIFO
D8
D9
D10
D11
D12
D13
D14
D15
ptr1,2
ptr3
from APPLICATION

Figure 50

Figure 51

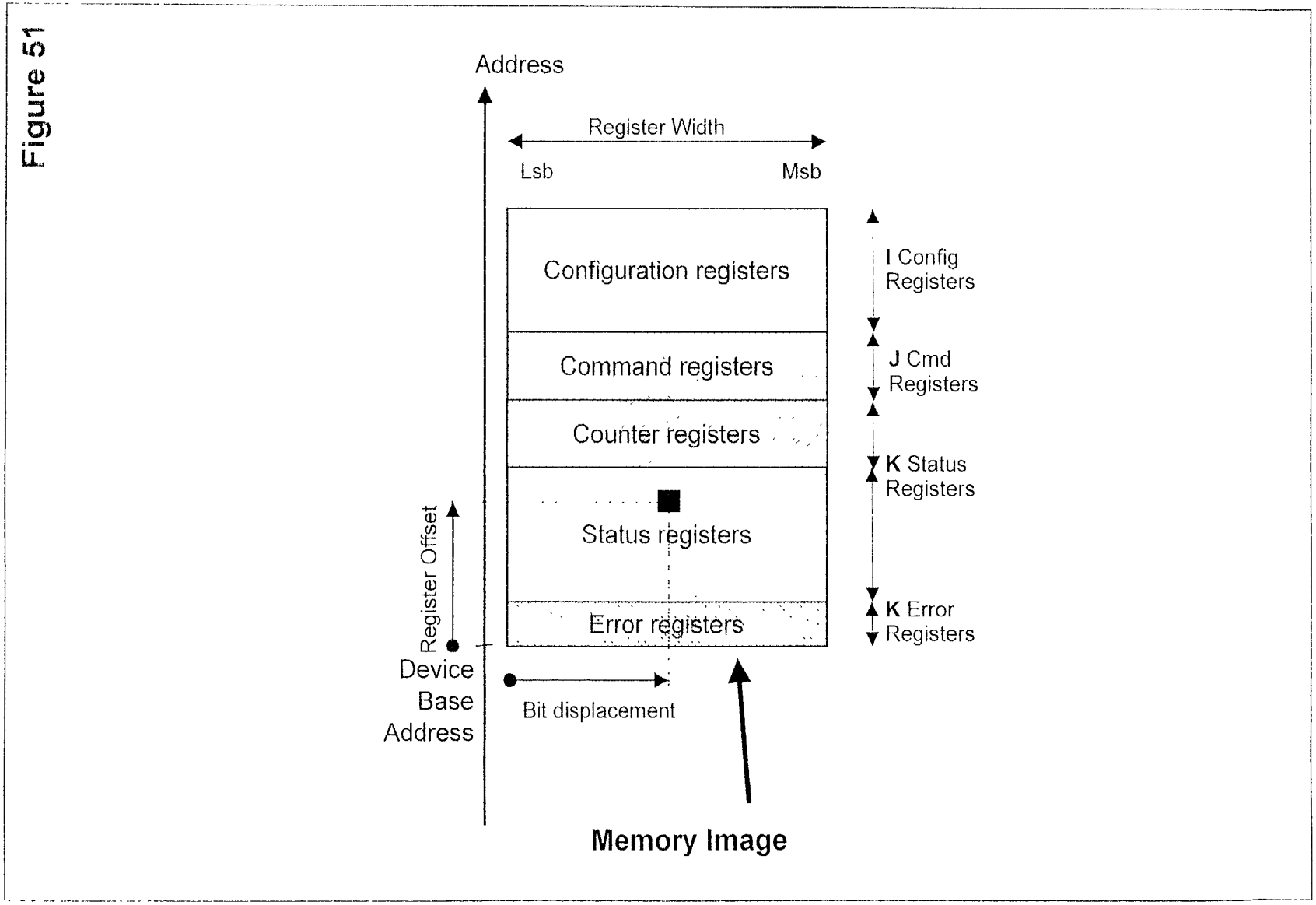

Address
Register Width
Lsb
Msb
Configuration registers
Command registers
Counter registers
Status registers
Error registers
I Config Registers
J Cmd Registers
K Status Registers
K Error Registers
Register Offset
Device Base Address
Bit displacement
Memory Image

Figure 52

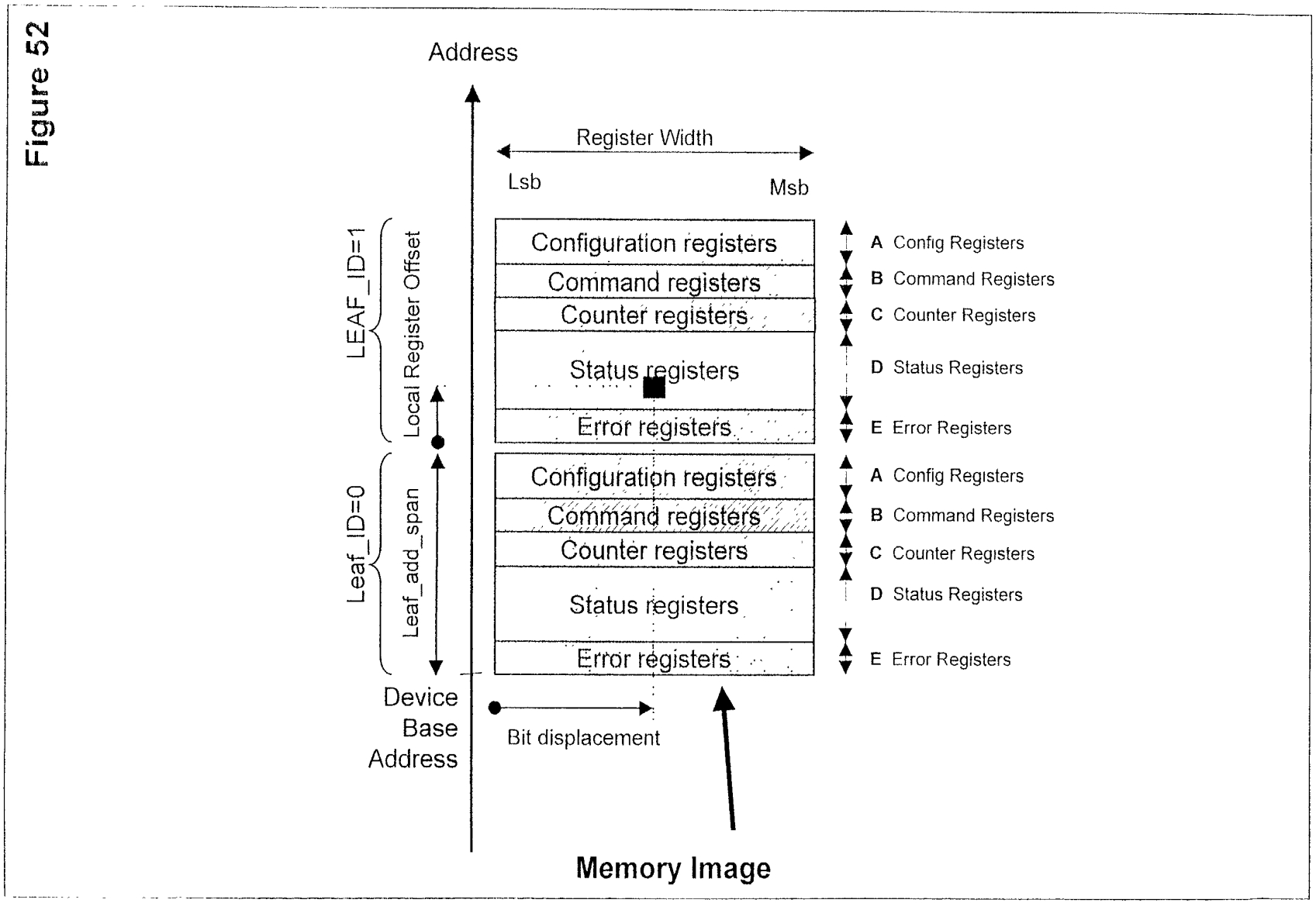

Address
Register Width
Lsb
Msb
LEAF_ID=1
Local Register Offset
Leaf_ID=0
Leaf_add_span
Configuration registers
Command registers
Counter registers
Status registers
Error registers
Configuration registers
Command registers
Counter registers
Status registers
Error registers
A Config Registers
B Command Registers
C Counter Registers
D Status Registers
E Error Registers
A Config Registers
B Command Registers
C Counter Registers
D Status Registers
E Error Registers
Device Base Address
Bit displacement
Memory Image

Figure 53

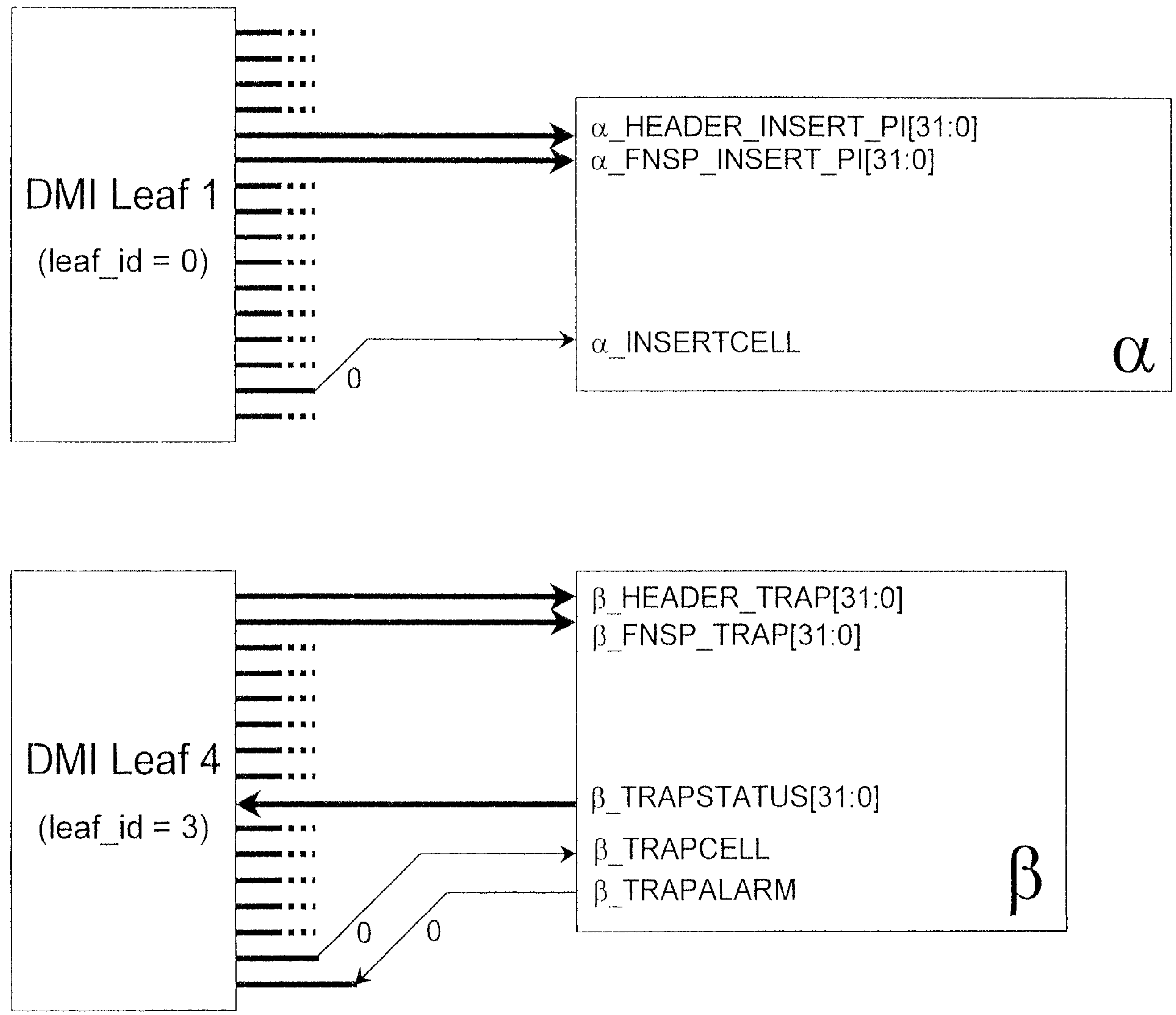

DMI Leaf 1
(leaf_id = 0)
α_HEADER_INSERT_PI[31:0]
α_FNSP_INSERT_PI[31:0]
α_INSERTCELL
α
0
DMI Leaf 4
(leaf_id = 3)
β_HEADER_TRAP[31:0]
β_FNSP_TRAP[31:0]
β_TRAPSTATUS[31:0]
β_TRAPCELL
β_TRAPALARM
β
0
0

Figure 54

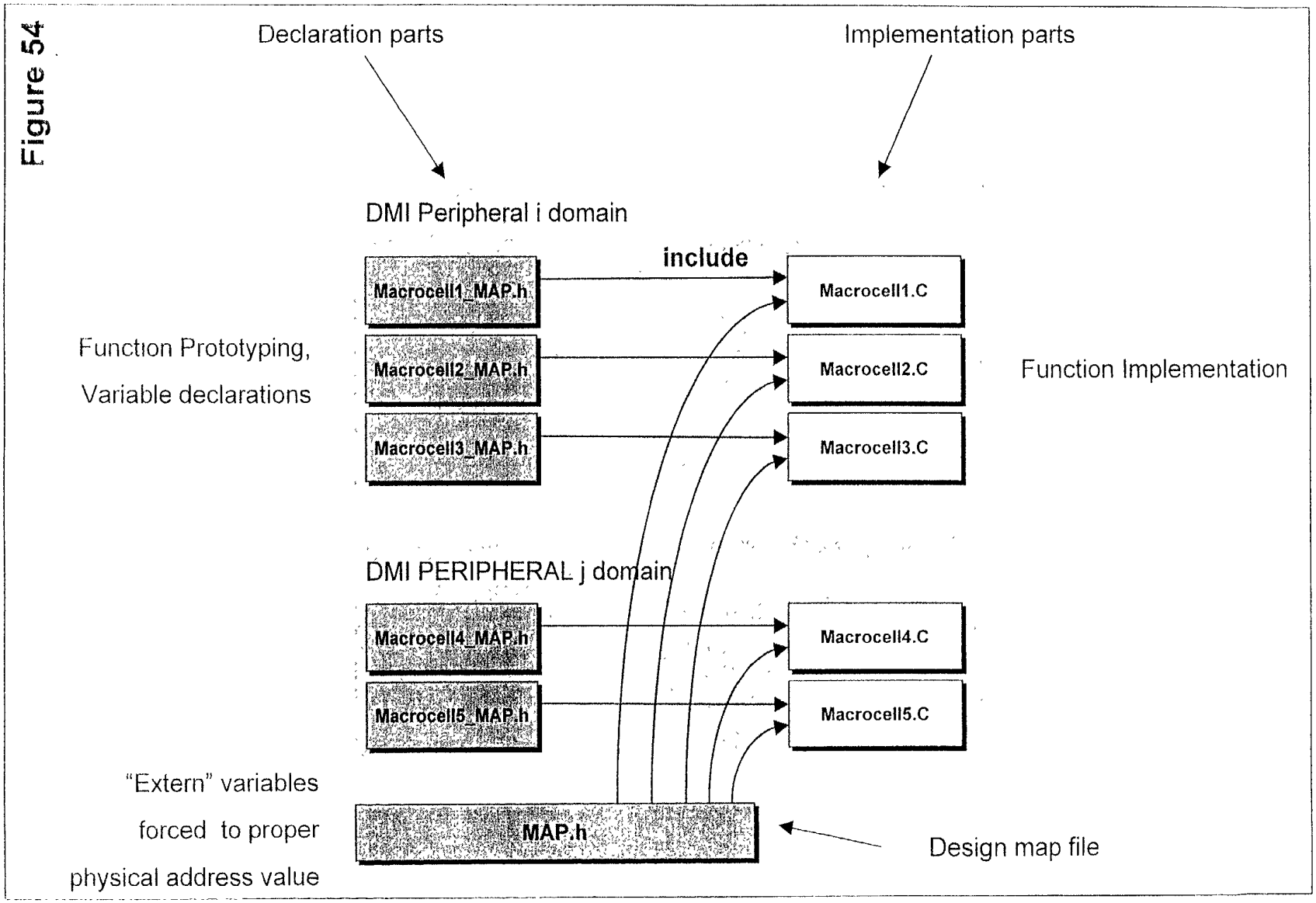
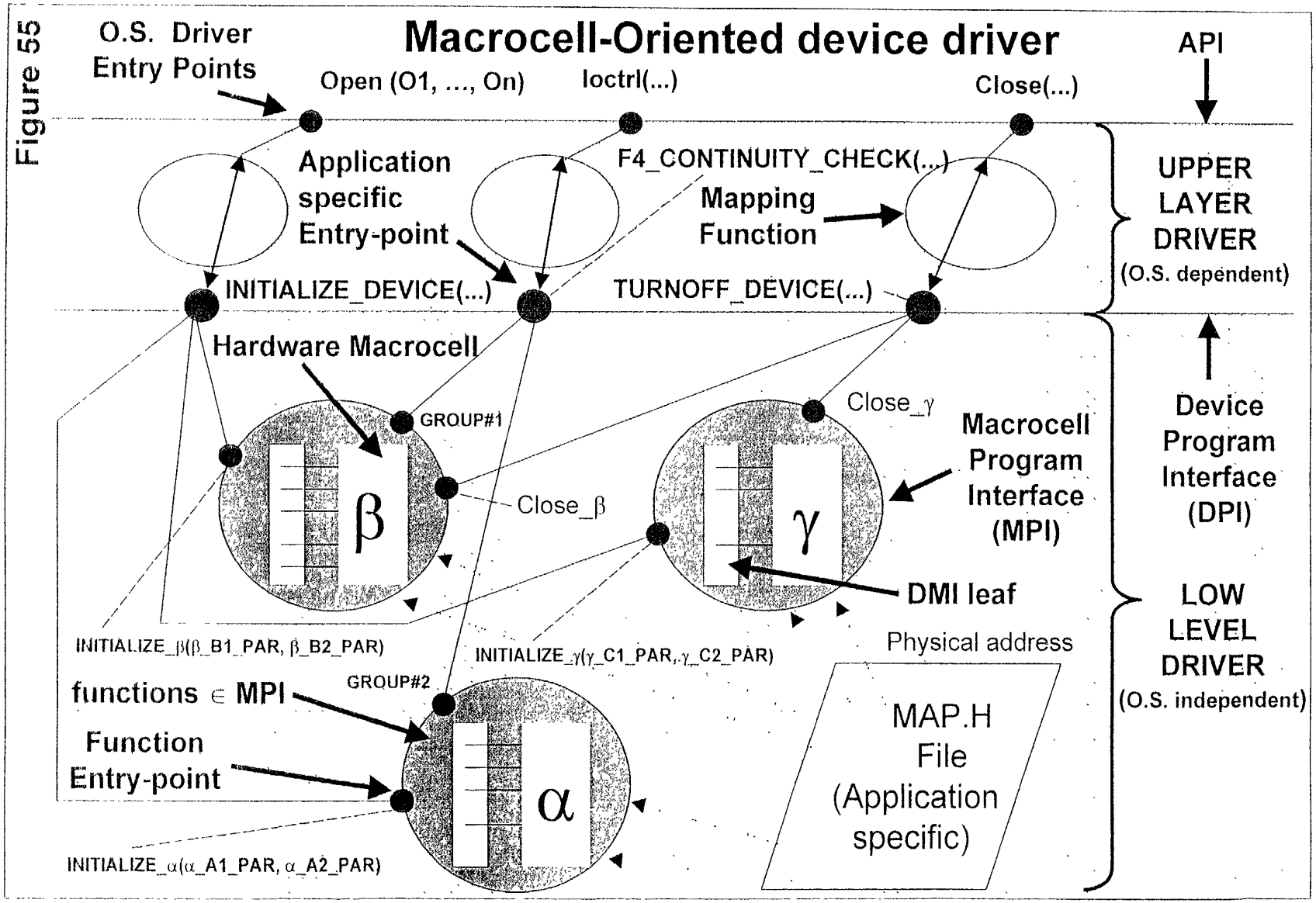

Declaration parts
Implementation parts
DMI Peripheral i domain
include
Macrocell1_MAP.h
Macrocell2_MAP.h
Macrocell3_MAP.h
Macrocell1.C
Macrocell2.C
Macrocell3.C
Function Prototyping,
Variable declarations
Function Implementation
DMI PERIPHERAL j domain
Macrocell4_MAP.h
Macrocell5_MAP.h
Macrocell4.C
Macrocell5.C
"Extern" variables
forced to proper
physical address value
MAP.h
Design map file

Figure 55


Macrocell-Oriented device driver
O.S. Driver Entry Points
Open (O1, ..., On)
Ioctrl(...)
Close(...)
API
Application specific Entry-point
F4_CONTINUITY_CHECK(...)
Mapping Function
UPPER LAYER DRIVER
(O.S. dependent)
INITIALIZE_DEVICE(...)
TURNOFF_DEVICE(...)
Hardware Macrocell
GROUP#1
Close_γ
Macrocell Program Interface (MPI)
Device Program Interface (DPI)
β
Close_β
γ
DMI leaf
LOW LEVEL DRIVER
(O.S. independent)
INITIALIZE_β(β_B1_PAR, β_B2_PAR)
INITIALIZE_γ(γ_C1_PAR, γ_C2_PAR)
Physical address
functions ∈ MPI
GROUP#2
Function Entry-point
α
MAP.H File (Application specific)
INITIALIZE_α(α_A1_PAR, α_A2_PAR)